Report

Task 4: Critical path of the circuit

This listing is produced using Timing analyzer, after placing and routing, based on auto-generated timing constraints.

Timming constraint: Default period analysis for net "clk_BUFGP"
107 paths analyzed, 41 endpoints analyzed, 0 failing endpoints
0 timing errors detected. (0 setup errors, 0 hold errors)
Minimum period is 3.234ns.

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Delay (setup path): 3.234 ns (data path - clock path skew + uncertainty)
Source: reg8/dout_sig_5 (FF)
Destination: reg8/dout_sig_5 (FF)
Data Path Delay: 3.199ns (Levels of Logic = 3)
Clock Path Skew: 0.000ns
Source Clock: clk_BUFGP rising
Destination Clock: clk_BUFGP rising
Clock Uncertainty: 0.035ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.070ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Maximum Data Path at Slow Process Corner: reg8/dout_sig_5 to reg8/dout_sig_5

<table>
<thead>
<tr>
<th>Location</th>
<th>Delay type</th>
<th>Delay(ns)</th>
<th>Physical Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLICE_X9Y4.CQ</td>
<td>Tcko</td>
<td>0.391</td>
<td>reg8/dout_sig&lt;5&gt;</td>
</tr>
<tr>
<td>SLICE_X10Y4.D4</td>
<td>net (fanout=4)</td>
<td>0.794</td>
<td>reg8/dout_sig&lt;5&gt;</td>
</tr>
<tr>
<td>SLICE_X10Y4.D</td>
<td>Tilo</td>
<td>0.203</td>
<td>reg8/dout_sig&lt;7&gt;</td>
</tr>
<tr>
<td>SLICE_X9Y4.D5</td>
<td>net (fanout=5)</td>
<td>0.406</td>
<td>Mmux_mux_o&lt;7:4&gt;421</td>
</tr>
<tr>
<td>SLICE_X9Y4.DMUX</td>
<td>Tilo</td>
<td>0.313</td>
<td>Mmux_mux_o&lt;7:4&gt;42</td>
</tr>
<tr>
<td>SLICE_X9Y4.G6</td>
<td>net (fanout=1)</td>
<td>0.770</td>
<td>N9</td>
</tr>
<tr>
<td>SLICE_X9Y4.CKL</td>
<td>Tas</td>
<td>0.322</td>
<td>reg8/dout_sig&lt;5&gt;</td>
</tr>
<tr>
<td>SLICE_X9Y4.CKL</td>
<td></td>
<td></td>
<td>Mmux_mux_o&lt;7:4&gt;2</td>
</tr>
<tr>
<td>SLICE_X9Y4.CKL</td>
<td></td>
<td></td>
<td>reg8/dout_sig&lt;5&gt;</td>
</tr>
</tbody>
</table>
Total 3.199ns (1.229ns logic, 1.970ns route) 
  (38.4% logic, 61.6% route)

Timing summary:
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Timing errors: 0  Score: 0  (Setup/Max: 0, Hold: 0)

Constraints cover 176 paths, 0 nets, and 108 connections

Design statistics:

Minimum period: 3.234ns{1}  (Maximum frequency: 309.215MHz)
Minimum input required time before clock: 2.288ns
Maximum output delay after clock: 7.224ns

Task 5: FPGA Resource Utilization After Implementation:

Number of occupied Slices: 7
Number of Slice LUTs: 17
Number of Slice Registers used as Flip-Flops: 15
Number of IO pins: 23

Slice Logic Utilization:

Number of Slice Registers: 15 out of 18,224 1%
Number used as Flip Flops: 15
Number used as Latches: 0
Number used as Latch-thrus: 0
Number used as AND/OR logics: 0
Number of Slice LUTs: 17 out of 9,112 1%
Number used as logic: 17 out of 9,112 1%
Number using O6 output only: 11
Number using O5 output only: 0
Number using O5 and O6: 6
Number used as ROM: 0
Number used as Memory: 0 out of 2,176 0%

Slice Logic Distribution:

Number of occupied Slices: 7 out of 2,278 1%
Number of MUXCYs used: 0 out of 4,556 0%
Number of LUT Flip Flop pairs used: 20
Number with an unused Flip Flop: 7 out of 20 35%
Number with an unused LUT: 3 out of 20 15%
Number of fully used LUT-FF pairs: 10 out of 20 50%
Number of slice register sites lost to control set restrictions: 0 out of 18,224 0%

IO Utilization:
Number of bonded IOBs: 23 out of 232 9%

Task 6: Minimum clock period and maximum clock frequency
Minimum period: 3.234 ns
Maximum frequency: 309.215 MHz