Lab Instructors:

Umar Sharif – Monday and Wednesday Section
Rabia Shahid – Thursday Section

Lab Sessions

Monday, 4:30-7:10pm, Engineering Building, room 3208
Wednesday, 7:20-10:00pm, Engineering Building, room 3208
Thursday, 7:20-10:00pm, Engineering Building, room 3208

Office Hours

Umar Sharif:
Monday, 12:00-1:00pm (priority given to ECE 448 students), ENGR 3204
Wednesday, 4:00-5:00pm (priority given to ECE 448 students), ENGR 3204
Thursday, 5:00-7:00pm (priority given to ECE 699 students), ENGR 3231

Rabia Shahid:
Tuesday, 4:00-6:00pm (priority given to ECE 332 students), ENGR 3203
Thursday, 2:00-4:00pm (priority given to ECE 448 students), ENGR 3204

Kris Gaj:
Monday, 3:00-4:00pm, ENGR 3225
Wednesday, 3:00-4:00pm, ENGR 3225
Thursday, 6:00-7:00pm, ENGR 3225

Web page

http://ece.gmu.edu → Courses → ECE 448
click on “FPGA and ASIC Design with VHDL”

Hardware Boards

We will use Digilent Nexys 3 FPGA Boards based on Spartan 6 FPGAs.
The boards will be distributed to students for free by the TAs during the lab sessions in
the fourth or fifth week of the semester. The boards should be returned to the TA during
the last lab sessions of the semester. In case the board you received appears to be out-of
order at the end of the semester, it will be your responsibility to replace it by a new board of the same type.

Additional equipment used during the labs may include oscilloscopes, logic analyzers, and prototyping boards.

**Software**

The following major CAD software will be introduced and used extensively in this class:

**At School:**

Aldec Active-HDL ver. 9.3  
Xilinx ISE Design Suite ver. 14.7

**At Home:**

Aldec Active-HDL Student Edition ver. 9.3 (free)  
Xilinx ISE/WebPACK ver. 14.7

**Assistance with the installation of software tools on your laptops will be provided during the first three lab sessions of the course on 01/26, 01/28 and 01/29.**

**Tutorials:**

Majority of tutorials used in this class is available at [http://ece.gmu.edu/tutorials-and-lab-manuals](http://ece.gmu.edu/tutorials-and-lab-manuals)

Please use "448" or "ECE 448" as a filter to see only the relevant materials.

**General Laboratory Rules**

- Each lab assignment will be preceded by an introduction and a hands-on session taught by a TA.

- The deadlines for submitting all lab deliverables (including source codes, diagrams, waveforms, configuration files, lab reports, etc.) are being set as follows:

  Monday section - Monday, 4:00 PM  
  Wednesday section - Wednesday, 7:00 PM  
  Thursday section - Thursday, 7:00 PM.
• Students will be required to demonstrate working experiment during a lab session on a day designated as a due date for a particular lab assignment.

• Experiment demonstrations will be accepted exclusively during the class time for a particular lab section.

• For each lab assignment, the demonstration and the electronic deliverables (including lab report) are each worth 50% of points allocated to a given lab assignment.

• Each lab assignment that is one week late will be penalized by deducting 1/3 of its allocated points. No credit will be received for a lab experiment that is more than one week late. Opportunities will be provided to earn bonus points by completing additional tasks for each assignment. Both penalty and bonus points will apply independently to the demonstrations and to the electronic deliverables.

• During the second part of the semester (after the Spring break), the students can follow one of the following two schedules:
  o Schedule A: Lab 4 - 2 weeks, Lab 5 - 2 weeks, Lab 6 - 2 weeks.
  o Schedule B: Lab 4 - 3 weeks, Lab 5 or Lab 6 - 3 weeks. **One lab is not attempted, and as a result its grade is set to 0.**
    o Schedule B is intended for students who feel that they fall behind, and need more time for Labs 4-6. These students can avoid late submission penalties, but at the same time, they have to give up their chance of earning points for one of the two last labs, Lab 5 or Lab 6. A decision about switching to Schedule B, should be communicated to the respective lab instructor no later than by the regular deadline for Lab 5 according to Schedule A.

• Students who do well in Labs 1-3 can sign up for Schedule A+. This schedule will involve working on an open-ended project proposed by the students, the TA, or the instructor. The project can be done individually or in groups of two students. The schedule of the project must include the following steps:
  o draft specification - Spring break week
  o revised specification approved by the instructor and the TA - 1 week
  o milestone 1 - 2 weeks
  o milestone 2 - 2 weeks
  o final report & deliverables - 1 week.

• Office hours will be devoted to helping students with their designs and answering any questions related to the subject of the course.

• Students are required to work individually on most assignments, unless group work is clearly stated in the text of the assignment. In case of group work, all
members of the team are expected to be intimately familiar with the entire solution to the given lab assignment and the entire lab report. This knowledge will be verified during the experiment demonstration and the same grade will be applied to the entire team.

• Every completed experiment must be presented to the TA, who will evaluate students' results and effort. It is the student's responsibility to convince the TA that their designs work as required. Therefore, students have to simulate and test their designs thoroughly and well document their work. The TA is not required to test anything by himself nor to investigate if the designs are correct in case of insufficient documentation.

• In order to prevent cheating and plagiarism, the students will be required to
  o submit all electronic deliverables using Blackboard at the designated time before the experiment demonstration,
  o restrain from any changes in the experiment files in the period between the electronic submission and the experiment demonstration,
  o answer correctly several detailed questions regarding their solution at the time of demonstration.
Not complying with either of these requirements may lead to either a total rejection of the demonstration by the TA, or to a substantial reduction of the number of points awarded to the student.

• In case of any evident attempt to submit somebody's else work as your own, both students involved in the incident may be penalized by taking away all points for the given lab assignment. **The two repeated attempts to present somebody's else work as your own may lead to the F grade for the entire course, independently of the total amount of points earned by the student before the second incident.**

• The students are encouraged to help and support each other in all problems related to the
  o operation of the CAD tools,
  o operation of the FPGA boards,
  o operation of the measurement equipment available in the lab,
  o understanding of the problem to be solved during each experiment.
Tentative Lab Schedule (subject to possible modifications):

1. Lab 0: Discussion of Lab Rules. Installation and Configuration of Tools. 01/26, 01/28, 01/29
2. Lab 1: Developing VHDL Testbenches
   Assigned: 01/26, 01/28, 01/29 Demonstrated: 1 week later
3. Lab 2: Combinational and Sequential Logic
   Assigned: 02/02, 02/04, 02/05 Demonstrated: 1 week later
4. Lab 3: State Machines. Using Basic Input/Output Devices. Assigned: 02/09, 02/11, 02/12 Demonstrated: 2 weeks later
5. Lab Midterm Exams
   03/02, 03/05
6. Lab 4: VGA Display
   Assigned: 03/16, 03/18, 03/19
   Demonstrated: 2 weeks later for Schedule A, 3 weeks later for Schedule B
7. Lab 5: Computer Graphics
   Assigned: 03/30, 04/01, 04/02 for Schedule A, 1 week later for Schedule B
   Demonstrated: 2 weeks later for Schedule A, 3 weeks later for Schedule B
8. Lab 6: PicoBlaze System
   Posted: 04/06, 04/08, 04/09 Discussed: 04/13, 04/15, 04/16
   Demonstrated: 04/27, 04/29, 04/030
9. Lab 7: Using Logic Analyzer (in class) 04/20, 04/22, 04/23

Students with Disabilities

If you need special assistance, please inform the instructor and the Office of Disability Services (ODS, http://ods.gmu.edu) as soon as possible. All special accommodations must be arranged through ODS.