Lecture 14

RTL Design Methodology

Part 1:

STATISTICS example
Structure of a Typical Digital System

Datapath (Execution Unit)

Data Inputs

Control Inputs

Datapath (Execution Unit)

Control (Control Unit)

Data Outputs

Control Outputs

Data Outputs

Status Signals

Control Signals
Hardware Design with RTL VHDL

Pseudocode

Datapath

Block diagram

VHDL code

Interface

Controller

ASM chart

VHDL code
Steps of the Design Process

1. Text description
2. Interface
3. Pseudocode
4. Block diagram of the Datapath
5. Interface divided into Datapath and Controller
6. ASM chart of the Controller
7. RTL VHDL code of the Datapath, Controller, and Top-Level Unit
8. Testbench for the Datapath, Controller, and Top-Level Unit
9. Functional simulation and debugging
10. Synthesis and post-synthesis simulation
11. Implementation and timing simulation
12. Experimental testing using FPGA board
Steps of the Design Process
Introduced in Class Today

1. Text description
2. Interface
3. Pseudocode
4. Block diagram of the Datapath
5. Interface divided into Datapath and Controller
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Class Exercise 1
STATISTICS
Pseudocode

```pseudocode
no_1 = no_2 = no_3 = sum = 0
wait for go
for i=0 to k-1 do
    sum = sum + din
    if din > no_1 then
        no_3 = no_2
        no_2 = no_1
        no_1 = din
    elseif (din > no_2) then
        no_3 = no_2
        no_2 = din
    elseif (din > no_3) then
        no_3 = din
    end if
end for
avr = sum / k
```
Circuit Interface

clk  reset  din  go

Statistics

done  dout  dout_mode
# Interface Table

<table>
<thead>
<tr>
<th>Port</th>
<th>Width</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>1</td>
<td>System clock.</td>
</tr>
<tr>
<td>reset</td>
<td>1</td>
<td>System reset.</td>
</tr>
<tr>
<td>din</td>
<td>n</td>
<td>Input Data.</td>
</tr>
<tr>
<td>go</td>
<td>1</td>
<td>Control signal indicating that the first input is ready.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Active for one clock cycle.</td>
</tr>
<tr>
<td>done</td>
<td>1</td>
<td>Signal set to high after the output is ready.</td>
</tr>
<tr>
<td>dout</td>
<td>n</td>
<td>Output dependent on the dout_mode input.</td>
</tr>
<tr>
<td>dout_mode</td>
<td>2</td>
<td>Control signal determining value available at the output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00: avr, 01: no_1, 10: no_2, 11: no_3.</td>
</tr>
</tbody>
</table>
STATISTICS: Solutions
Block diagram of the Datapath
Interface with the division into the Datapath and Controller

Datapath

- din
- dout_mode
- clk
- reset
- n
- 2
- dout

Controller

- go
- en1
- en2
- en3
- esum
- enc
- s2
- s3

done
ASM Chart of the Controller