Draw a detailed block diagram of the digital system including

1. the PicoBlaze-6 core, KCPSM6
2. the instruction ROM required for the basic operation of the PicoBlaze core
3. 64 x 8 external data RAM visible under addresses 0x00-0x3F
4. 64 x 8 external data ROM visible under addresses 0x40-0x7F
5. two input registers with the virtual addresses 0x80 and 0xCF
6. two output registers with the virtual addresses 0x80 and 0xC0
7. a D flip-flop with the output Q connected to the interrupt input of the PicoBlaze core, input SET connected to the external port INT, and input CLR connected to an appropriate output of the PicoBlaze core.

Assume that

- input register with the address 0x80 is the same as the output register with the address 0x80
- the input and output registers, data RAM, and data ROM specified above are the only i/o devices that the PicoBlaze core is communicating with
- your system needs to be able to allow the PicoBlaze core to write to all aforementioned output registers and data RAM, and read from all the aforementioned input registers, data RAM, and data ROM, using instructions OUTPUT and INPUT, respectively
- you need to provide all details of the address decoder, and build it out of basic logic components you are familiar with
- all registers and flip-flops have a reset input connected to the external port RESET.

Please clearly mark on your schematic:

- sizes of all memories and registers
- sizes and directions of all buses.