Homework 1  
due Monday, February 6, 2012, 7:20pm

Task 1

Draw detailed diagrams showing how the following operations can be efficiently implemented using internal resources of Xilinx Spartan 3 FPGAs:

a. addition
   \[(Cout, S)=X+Y\]
b. increment
   \[(Cout, S)=X+1\]
c. decrement
   \[(Cout, S)=X-1\]
d. three-operand addition
   \[(Cout, S)=X+Y+Z.\]

Assume that
- X, Y, Z, and S are 5-bit long.
- Cout is a single bit.
- All circuits are purely combinational.

Clearly show which parts of your circuit are implemented using LUTs, and which using hardwired resources of Carry & Control logic. Clearly write an equation for a function implemented by each LUT or draw a corresponding circuit inside of a LUT box.

Based on these diagrams determine how many LUTs and how many Logic Cells (1/2 of a CLB slice) are required to perform these operations.

Task 2

Develop generic k-bit versions of operations specified in Task 1 in VHDL. Use the “+” operator of VHDL, and std_logic_vector type for X, Y, Z, and S. Do not build adders out of Full Adders and/or Half-Adders.

Develop generic k-bit wrappers that surround the combinational circuits listed above and store each input and output in a register.

Task 3

Synthesize and implement your circuit for the following values of the generic k:

\[k=5 \text{ and } k = 2^i \text{ for } i=4..9,\]

targeting Xilinx Spartan 3 FPGAs. Use the smallest device of the Spartan 3 family capable of holding the three-operand adder for \(k=2^9=512.\)
When determining circuit area (measured in CLB slices), synthesize and implement your circuit without any surrounding registers.

When determining minimum clock periods, synthesize and implement your circuit with surrounding input/output registers. Assume that the delay of each investigated circuit is equal to the minimum clock period obtained from your implementation.

**Task 4**

Based on the actual resource utilization and the analysis of critical paths for the aforementioned circuits with \( k=5 \), verify whether your diagrams developed in Task 1 are correct.

If you see any disagreements, try to explain them, and if needed redraw diagrams proposed in Task 1.

**Task 5**

Create tables and draw diagrams showing delay and resource utilization (in CLB slices) of all aforementioned circuits as a function of \( k \), with \( k = 2^i \) for \( i=4..9 \).

For each circuit, verify the hypothesis, that the delay and area can be described using affine functions of the form:

\[
\text{Delay}(k) = d_0 + k \cdot d_1 \\
\text{Area}(k) = a_0 + k \cdot a_1.
\]

If this hypothesis holds, find values of constants \( d_0, d_1, a_0, \) and \( a_1 \) for each of the investigated circuits.

Analyze your results, and describe your observations and conclusions in the final report.

**Bonus Task 1**

Repeat Tasks 3-5 for Xilinx Spartan 6 or Xilinx Virtex 5. Compare the obtained results with results obtained using Spartan 3.

**Bonus Task 2**

Repeat Tasks 3-5 for Altera Cyclone III or Altera Stratix III. Compare the obtained results with results obtained using Spartan 3.

**Deliverables:**

1. Diagrams (hand-drawn or drawn using graphical editor, such as Xfig)
2. Source codes