1 Introduction

This pre-lab consists of two parts. Part one will help familiarize yourself with the basic logic gates. Part two of the pre-lab consists of general questions regarding VHDL.

2 Basic Logic Gates

In lab two you will explore the function of the basic gates. In preparation for this review the operation of the basic gates. Complete the following truth tables and draw the schematic symbol of each gate.
3 Short Questions

What is an Entity?

What is an Architecture?

Why do we include the statement
Library ieee;

Why do we include the statement
use ieee.std_logic_1164.all;

What is a "signal" in VHDL?

What are the different data types we can use in VHDL? Give their respective ranges?
What is the purpose of a test bench?