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Aldec Active-HDL Tutorial

Introduction

This document is intended to assist ECE students taking ECE 448, FPGA and ASIC design with VHDL in setting up their computing environment for using Aldec tools.

Active-HDL is an integrated environment designed for development of VHDL designs. The core of the system is a VHDL simulator. Along with debugging and design entry tools, it makes up a complete system that allows you to write, debug and simulate VHDL code. Based on the concept of a design, Active-HDL allows you to organize your VHDL resources into a convenient and clear structure.

Students can use Active-HDL to perform following tasks:

- development of the VHDL based designs
- functional simulation of their code
- functional simulation of the synthesized code
- timing simulation of the hardware implementation

Objective

This tutorial helps you to

- Download and Install Aldec Active-HDL.
- Create a new design or add .vhd files to your design.
- Compile and debug your design.
- Perform simulation.
Start-up

1. Double click on the Active-HDL icon on the desktop; it comes up with a “getting started” window.

   a. Select “Create new workspace” and click “OK”. This creates a new workspace in your directory.
   b. Selecting “Open existing workspace” gives you the option to choose from your previous workspaces.
   c. If “Always open last workspace” is checked, Active-HDL will default by opening the last open workspace.

2. Type the desired workspace name and click “OK.” The default location for your workspace is “c:/my_designs”.

   ![Getting Started](image_url)
   ![New Workspace](image_url)
3. Select “Create an empty design.” This creates a new design in your workspace. Click “Next” to continue.

4. Choose “Default HDL Language” as the “Block Diagram Configuration” and “VHDL” as your “Default HDL Language.” Click “Next.”
5. Type the design name you would like to create and click the “Next” tab. Your default location will be “c:/my_designs/{workspace name}.”

6. Design name and design directory will now be displayed. Verify that this information is correct. Proceed by clicking “Finish.”
7. You should now be at the following screen.
Adding VHDL source files

1. To add existing source files, click on “Add New File.” Then select “Add Files to Design.”

2. To create a new source file, click “Add New File > New > VHDL Source.”

3. New VHDL source files can also be created by selecting “File > New > VHDL Source.”
4. Click “Next” on the new source file wizard.

5. Type the name of the source file that you would like to create; you will be able to choose a new name for each entity. If you wish, you may also choose a name for the architecture. If not, the default architecture name will be your entity name.
6. Select “New” in the “New source File Wizard-Ports” window. You can start declaring your inputs and outputs by repeating this step. When all of the ports have been named, click “Finish.”

7. If you have multiple designs in the same workspace, you will need to set an active design. This can be done by Right-Clicking on your design and select “Set as Active Design.”
Compiling the Design

1. Once all of the files are added to the design, it can be complied. There are three ways to do this:
   a. Clicking on the toolbar (shown below).
   b. Press F11.
   c. Click “Design > Compile.”

2. The Console Window (located at the bottom of the screen) will give the output to the compile command. The image below shows success. If there were compile errors, they would also be listed here.

Generating Testbench

1. To add your existing testbench, follow the instructions above for adding existing files.
2. To generate a new testbench, click “Tools > Generate Testbench.”
3. Under Entity, select the entity that you would like to create the testbench for. The particular architecture being tested can be selected under “Architecture.” Select “Single Process” as the Test Bench Type and click “Next” to continue.

4. The test bench generator wizard appears with all of your input ports under “UUT ports.” Click “Next” to continue.
5. Enter the names of the entity, architecture, and source file or accept the default names chosen by Active-HDL. Click “Next.”

6. Verify that all of the file information is correct and click “Finish” to generate the test bench.
NOTE: Add your test conditions to the Testbench, Hit F11 to compile.

Getting Started with the Simulation

1. Compile the design (See above).
2. Before starting the simulation, select the test bench as your “Top Level” unit (see below).
3. Initialize the simulation by clicking “Simulation > Initialize Simulation.”
4. Click “Structures” to see all of the ports. Add desired signals to waveform as shown below.
5. Press F5 or click “Simulation > Run For” to simulate.

Wave Window Toolbar

1. “Zoom in” causes the current visible waveform window to cover less time. This has the effect of spreading the signals.
2. “Zoom out” causes the current visible waveform window to cover more time. This allows more events to be observed.
3. “Zoom to Fit” adjusts the visible window to cover the span of time that has currently been simulated.
4. “Add signals” allows more signals to be added to the current waveform.