1. How many data words of the size of 32 bits can be held in a single Block RAM in Spartan 6 FPGA?

512

How many parity bits can accompany each data word?

4

2. Based on your knowledge of the internal structure of the Spartan 6 FPGAs, and assuming that
   A. The Debouncer circuit shown in Figs. 1 and 2 is implemented using CLB slices only,
   B. Generics k and DD have the following values: $k=24$, $DD = 10,000,000$,
   perform the following tasks:

   a. **In the diagrams below**, please circle any portion of logic that can be implemented using:
      - n Multipurpose Look-up Tables – MLUTs, or
      - n Storage Elements – SE,
      where $n \geq 1$.
   b. Next to each circle write
      - n MLUT, $<\text{MLUT\_mode}>$, or
      - n SE, $<\text{SE\_mode}>$,
      where
      - n is the number of the respective FPGA structures (MLUTs or SEs), and
      - $<\text{MLUT\_mode}> = \text{ROM}$ (logic), RAM, or SR (shift register),
      - $<\text{SE\_mode}> = \text{FF}$ (flip-flop) or LT (latch).
   c. For the arithmetic components, implemented using Carry Logic, please circle these components, and write next to them
      - n (CL+MLUT),
      where n is the number of the Carry Logic stages used.

**Hint:** One Carry Logic stage and one associated MLUT can be used to implement one Full Adder.
Fig. 1: Implementation of the Counter in the Debouncer circuit.

Fig. 2: Block diagram of the Debouncer circuit.
3. Fill in the blanks in the following code describing the circuit shown below:

Circuit

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY Example1 IS
PORT (w : IN STD_LOGIC_VECTOR(0 TO 15);
      s : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
      f : OUT STD_LOGIC);
END Example1;
ARCHITECTURE structural OF Example1 IS
COMPONENT mux4to1
  PORT (w0, w1, w2, w3 : IN STD_LOGIC;
        s   : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
        f   : OUT STD_LOGIC);
END COMPONENT;

  SIGNAL m : STD_LOGIC_VECTOR(0 TO 3);
BEGIN
  G1: FOR i IN 0 TO 3 GENERATE
      Muxes: ............... PORT MAP (w0, w1, w2, w3, s(1 downto 0), m(i));
    END GENERATE;
  Mux5: ............... PORT MAP (m(0), m(1), m(2), m(3),
                                f);
END structural;

4. For the VHDL code given below, perform the following TWO tasks
   a. Supplement the code with the proper contents of the sensitivity list
   b. Draw a block diagram of the corresponding digital circuit

process(video_on, wall_on, bar_on, sq_ball_on, wall_rgb, bar_rgb, ball_rgb)
begin
  if video_on='0' then
    graph_rgb <= "000"; --blank
  else
    if wall_on='1' then
      graph_rgb <= wall_rgb;
    elsif bar_on='1' then
      graph_rgb <= bar_rgb;
    elsif sq_ball_on='1' then
      graph_rgb <= ball_rgb;
    else
      graph_rgb <= "110"; -- yellow background
    end if;
  end if;
end process;