ECE 448
FPGA and ASIC Design with VHDL
Spring 2019
Kris Gaj

Research and teaching interests:

• reconfigurable computing
• cryptography
• computer arithmetic
• high-level synthesis

Contact:

The Engineering Building, room 3225
kgaj@gmu.edu
Course Web Page

Google “Kris Gaj” →

ECE 448 FPGA and ASIC Design with VHDL
TAs

Viet Dang
Ph.D. Student
Member of the Cryptographic Engineering Research Group (CERG) since August 2017

Joseph Prince Mathew
MSEE Student
Doing MS Thesis with Dr. Zhang
Computer Engineering Progression of Core Courses

This is not a suggested schedule. It only illustrates dependencies and shows courses in earliest possible semester.

Not all courses required for the degree are shown.

1) Math 203 can be taken concurrently with ECE 220
2) Requires completion of 45 credits
3) Requires completion of 90 credits applicable to your major

<table>
<thead>
<tr>
<th>Prerequisite</th>
<th>Co–Requisite</th>
<th>Co–Requisite +</th>
<th>Semester</th>
</tr>
</thead>
<tbody>
<tr>
<td>Must be taken in sequence</td>
<td>Should be taken concurrently but not earlier</td>
<td>Suggested to be taken in sequence</td>
<td>Courses between dashed lines can be taken concurrently</td>
</tr>
</tbody>
</table>

Catalog Year 2018/2019
Electrical Engineering Progression of Core Courses

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Must be taken in sequence

Co–Requisite
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Co–Requisite +
Suggested to be taken in sequence

Semester
Courses between dashed lines can be taken concurrently

Catalog Year 2018/2019
Digital system design technologies coverage in the CpE & EE programs at GMU

- **Microprocessors**
  - ECE 445: Computer Organization
  - ECE 447: Single Chip Microcomputers

- **FPGAs**
  - ECE 448: FPGA and ASIC Design with VHDL

- **ASICs**
  - ECE 431: Digital Circuit Design

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- **Microprocessors**
  - ECE 511: Advanced Microprocessors
  - ECE 611: Microprocessors

- **Real-Time Embedded Systems**
  - ECE 612: Real-Time Embedded Systems

- **Software/Hardware Codesign**
  - ECE 615: Software/Hardware Codesign

- **Digital System Design with VHDL**
  - ECE 545: Digital System Design with VHDL

- **Computer Arithmetic**
  - ECE 645: Computer Arithmetic

- **Digital Integrated Circuits**
  - ECE 586: Digital Integrated Circuits

- **VLSI Design for ASICs**
  - ECE 681: VLSI Design for ASICs
Course Hours

Lecture:

Monday, Wednesday
1:30-2:45 PM, Innovation Hall, room 204

Lab Sessions:

Tuesday
9:00-11:40 AM

Wednesday
7:20-10:00 PM

Friday
8:30-11:20 AM

The Nguyen Engineering Bldg., room 3208
General Section Assignment Rules

• You should do your best to attend all lab meetings of the section you are registered for.

• If you have missed a meeting of your section please attend a meeting of another section, but give preference in access to the lab computers to the students attending their own lab section.

• All lab assignment demos should be normally done exclusively during the class time of your section.

• Any requests for exceptions to these rules (due to illness, accident, etc.) should be well documented and presented to the TA & primary instructor for approval.
Office Hours

You are welcome to attend all office hour sessions! You can direct your questions regarding lab assignments to the TA and the instructor.

Do your best to avoid “chasing” the TAs outside of their office hours! They have other important and often urgent work to do!

Viet Dang
- Monday, 4:30-5:30pm, ENGR 3208
- Tuesday, 3:00-4:00pm, ENGR 3208

Joseph Prince Mathew
- Thursday, 11:00am-1:00pm, ENGR 3208

Kris Gaj
- Monday, 3:00-4:00pm, ENGR 3225
- Wednesday, 3:00-4:00pm, ENGR 3225
Getting Help Outside of Office Hours

piazza

• System for asking questions 24/7
• Answers can be given by students and instructors
• Student answers endorsed (or corrected) by instructors
• Average response time in Spring 2018 = 1.1 hour
• You can submit your questions anonymously
• You can ask private questions visible only to the instructors
Lab Access Rules and Behavior Code

Please refer to

ECE Labs website

and in particular to

Access rules & behavior code
# Course Web Page

http://ece.gmu.edu/coursewebpages/ECE/ECE448/S19

<table>
<thead>
<tr>
<th>Organization</th>
<th>Lecture</th>
<th>Lab</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instructor</td>
<td>Textbooks</td>
<td>Rules</td>
</tr>
<tr>
<td>Teaching Assistants</td>
<td>Lecture Slides</td>
<td>Lab Assignments</td>
</tr>
<tr>
<td>Lecture and Lab Time</td>
<td>Homework</td>
<td>Lab Slides &amp; Examples</td>
</tr>
<tr>
<td>Office Hours</td>
<td>Past Quizzes</td>
<td>Software</td>
</tr>
<tr>
<td>Grading</td>
<td>Past Midterm Exams</td>
<td>Hardware</td>
</tr>
<tr>
<td></td>
<td>Past Final Exams</td>
<td>Useful References</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Past Lab Exams</td>
</tr>
</tbody>
</table>
Grading criteria

First part of the semester (before the Spring break)

Lab experiments - Part I
16%

Lab exercises – Part I
1.6%

Quizzes & homework: 3%

Midterm exam for the lecture: 10%
Midterm exam for the lab: 15%

Second part of the semester (after the Spring break)

Lab experiments - Part II
24%+2%

Lab exercises – Part II
2.4%

Quizzes & homework: 3%

Final exam
25%
Tentative Grading Scheme for the Labs

Lab 1: Developing VHDL Testbenches – 4 points
Lab 2: Combinational & Sequential Logic – 4 points
Lab 3: State Machines. Basic I/O Devices. – 8 points

Total: 16 points

Lab 4: VGA Display – 8 points
Lab 5: MicroBlaze – Part 1 – 8 points
Lab 6: MicroBlaze – Part 2 – 8 points
Lab 7: Logic Analyzer (in class) – 2 bonus points

Total: 24+2 points
Penalties and Bonus Points

Penalties:

one-week delay: \( \frac{1}{3} \) of points

i.e., you can earn max. 4 out of 6 points

No submissions or demos will be accepted more than one week after the assignment is due!

Bonus points:

Majority of labs will have opportunities for earning bonus points by doing additional tasks
Flexibility in the Second Part of the Semester

Schedule A:

Lab 4: VGA Display (2 weeks) – 8 points
Lab 5: MicroBlaze – Part 1 (2 weeks) – 8 points
Lab 6: MicroBlaze – Part 2 (2 weeks) – 8 points
Lab 7: Logic Analyzer (in class) – 2 bonus points

Total: 24+2 points

Schedule B:

Lab 4: VGA display (3 weeks) – 8 points
Lab 5: MicroBlaze – Part 1 (3 weeks) – 8 points
Lab 7: Logic Analyzer (in class) – 2 bonus points

Total: 16+2 points
Flexibility in the Second Part of the Semester

Schedule A+:

• Intended for students who do very well in the first part of the semester (preferably ≥ 90% of points for Labs 1-3)

• An open-ended project proposed by students, the TAs, or the instructor

• Can be done individually or in groups of two students

• Schedule:  
  Detailed Specification  (1 week)
  Milestone 1  (2 weeks)
  Milestone 2  (2 weeks)
  Final Report & Deliverable  (1 week)

Total: 25 points
## Bonus Points for Class & Piazza Activity

- Based on class exercises during lecture and lab sessions, as well as your answers to other student’s questions on Piazza
- “Small” points earned each week posted on BlackBoard
- Up to 5 “big” bonus points
- Scaled based on the performance of the best student

For example:

<table>
<thead>
<tr>
<th></th>
<th>Small points</th>
<th>Big points</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Alice</td>
<td>40</td>
<td>5</td>
</tr>
<tr>
<td>2. Bob</td>
<td>32</td>
<td>4</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>26. Zach</td>
<td>8</td>
<td>1</td>
</tr>
</tbody>
</table>
Exams

• Midterm Exam for the Lecture – 10 points
  Wednesday, February 27

• Midterm Exam for the Lab (hands-on) – 15 point
  Tuesday, March 5
  Wednesday, March 6
  Friday, March 8

• Final Exam – 25 points
  Wednesday, May 8, 1:30-4:15pm
  (first day of the exam session)
Required Textbook

Supplementary Textbook – Basics Refresher

Supplementary Textbook – Advanced

ECE 448, FPGA and ASIC Design with VHDL

Topics

**VHDL:**
- writing testbenches
- writing synthesizable RTL level code in VHDL

**FPGAs:**
- architecture of FPGA devices
- embedded resources (memories, DSP units)
- tools for the computer-aided design with FPGAs
- current FPGA families & future trends
Applications:
- basics of computer arithmetic
- applications from communications, computer vision, cryptography, etc.

Platforms & Interfaces:
- FPGA boards
- I/O modules (VGA controller, serial communication modules)

New Trends:
- microprocessors embedded in FPGAs (MicroBlaze, ARM)
- using high-level programming languages to design hardware

High-level ASIC Design:
- standard cell implementation approach
- logic synthesis tools
- differences between FPGA & standard-cell ASIC design flow
Tasks of the course

Advanced course on digital system design with VHDL
- writing VHDL code for synthesis
- design using division into the datapath & controller
- testbenches

Comprehensive introduction to FPGA & front-end ASIC technology
- hardware:
  Xilinx FPGAs,
  Library of standard ASIC cells
- software:
  VHDL simulators,
  Synthesis tools,
  Implementation tools

Testing equipment
- oscilloscopes
- logic analyzer
VHDL for Specification

VHDL for Simulation

VHDL for Synthesis
Levels of design description

- Algorithmic level
- Register Transfer Level
- Logic (gate) level
- Circuit (transistor) level
- Physical (layout) level

Levels supported by HDL:

- Level of description most suitable for synthesis
Register Transfer Level (RTL) Design Description

Combinational Logic

Registers

Combinational Logic
What is an FPGA?

- Block RAMs
- Configurable Logic Blocks
- I/O Blocks
- Block RAMs
Modern FPGA

(#Logic resources, #DSP units, #RAM_blocks)

Graphics based on The Design Warrior’s Guide to FPGAs
Devices, Tools, and Flows. ISBN 0750676043
Copyright © 2004 Mentor Graphics Corp. (www.mentor.com)
General structure of an FPGA

Programmable interconnect

Programmable logic blocks
Two competing implementation approaches

ASIC
Application Specific Integrated Circuit

- designed all the way from behavioral description to physical layout
- designs must be sent for expensive and time consuming fabrication in semiconductor foundry

FPGA
Field Programmable Gate Array

- no physical layout design; design ends with a bitstream used to configure a device
- bought off the shelf and reconfigured by designers themselves
FPGAs vs. ASICs

**ASICs**

- High performance
- Low power
- Low cost (but only in high volumes)

**FPGAs**

- Off-the-shelf
- Low development costs
- Short time to the market
- Reconfigurability
Design and implement a simple unit permitting to speed up encryption with RC5-similar cipher with fixed key set on 8031 microcontroller. Unlike in the experiment 5, this time your unit has to be able to perform an encryption algorithm by itself, executing 32 rounds. .

Library IEEE;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity RC5_core is
  port (clock, reset, encr_decr: in std_logic;
        data_input: in std_logic_vector(31 downto 0);
        data_output: out std_logic_vector(31 downto 0);
        out_full: in std_logic;
        key_input: in std_logic_vector(31 downto 0);
        key_read: out std_logic;
        k);
end AES_core;

Specification (Lab Assignments)

On-paper hardware design
(Block diagram & ASM chart)

VHDL description (Your Source Files)

Functional simulation

Synthesis

Post-synthesis simulation
FPGA Design process (2)

- Implementation
- Configuration
- Timing simulation
- On chip testing
FPGA Boards
<table>
<thead>
<tr>
<th>Callout</th>
<th>Component Description</th>
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<th>Component Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power good LED</td>
<td>9</td>
<td>FPGA configuration reset button</td>
</tr>
<tr>
<td>2</td>
<td>Pmod port(s)</td>
<td>10</td>
<td>Programming mode jumper</td>
</tr>
<tr>
<td>3</td>
<td>Analog signal Pmod port (XADC)</td>
<td>11</td>
<td>USB host connector</td>
</tr>
<tr>
<td>4</td>
<td>Four digit 7-segment display</td>
<td>12</td>
<td>VGA connector</td>
</tr>
<tr>
<td>5</td>
<td>Slide switches (16)</td>
<td>13</td>
<td>Shared UART/ JTAG USB port</td>
</tr>
<tr>
<td>6</td>
<td>LEDs (16)</td>
<td>14</td>
<td>External power connector</td>
</tr>
<tr>
<td>7</td>
<td>Pushbuttons (5)</td>
<td>15</td>
<td>Power Switch</td>
</tr>
<tr>
<td>8</td>
<td>FPGA programming done LED</td>
<td>16</td>
<td>Power Select Jumper</td>
</tr>
</tbody>
</table>
FPGA Tools
Xilinx ISE
Integrated Software Environment
(not used this semester)

• Older development environment
• Frozen at version 14.7 in 2012 (although new releases of v14.7 still posted periodically)
• Replaced by Xilinx Vivado for the new FPGA families, starting at Series-7 FPGAs (Artix-7, Kintex-7, Virtex-7)
• Used in ECE 448 until 2017
Support for Xilinx Families

<table>
<thead>
<tr>
<th>Technology</th>
<th>Family</th>
</tr>
</thead>
<tbody>
<tr>
<td>90 nm</td>
<td>Spartan-3, Virtex-4</td>
</tr>
<tr>
<td>65 nm</td>
<td>Virtex-5</td>
</tr>
<tr>
<td>45 nm</td>
<td>Spartan-6</td>
</tr>
<tr>
<td>40 nm</td>
<td>Virtex-6</td>
</tr>
<tr>
<td>28 nm</td>
<td>Artix-7, Kintex-7, Virtex-7</td>
</tr>
<tr>
<td>20 nm</td>
<td>Kintex-7 UltraSCALE, Virtex-7 UltraSCALE</td>
</tr>
<tr>
<td>16 nm</td>
<td>Kintex-7 UltraSCALE+, Virtex-7 UltraSCALE+</td>
</tr>
</tbody>
</table>

Future Families
Vivado Design Suite
(used for the first time in Spring 2018)

• 4 years of development and 1 year of beta testing
• first version released in Summer 2012
we will use version 2017.2
• scalable data model, supporting designs with up to 100 million ASIC gate equivalents (GEs)
• Support for VHDL-2008
• Support for High-Level Synthesis
Vivado HLS

High Level Language
C, C++, System C

Vivado HLS

Hardware Description Language
VHDL or Verilog
Productivity Gains

- Vivado Simulator *3x faster than ISim*
- Synthesis *3x faster than Xilinx XST* (part of ISE)
- Substantial improvement in runtime and maximum design size compared to Xilinx ISE
- Much better visibility into key design metrics, such as timing, power, resource utilization, and routing congestion much earlier during the design process
- Estimates becomes progressively more accurate
Additional Simulation Tool

ModelSim

ModelSim-Intel FPGA Starter Edition

ModelSim:
• Industry standard for simulation
• Significantly faster than Vivado Simulator
• Windows, Linux OS
• Mixed-language support: VHDL, Verilog, System Verilog
• Recommended for advanced users

Features of the Starter Edition:
• Free, no license required
• 10,000 executable line limit
Why ECE 448 is a challenging course?

- need to refresh and strengthen your VHDL skills
- need to learn new tools
- need to perform practical experiments
- time needed to complete experiments
Difficulties
(based on a student survey)

• finding time to do the labs – 15

• learning VHDL – 2

• getting used to software – 1
Self-evaluation
(based on a student survey)

8 – worse than expected
16 – as well as expected
3 – better than expected
Why is this course worth taking?

• **VHDL** for synthesis: one of the most sought-after skills

• knowledge of state-of-the-art **tools** used in the industry

• knowledge of the modern **FPGA & ASIC technologies**

• knowledge of state-of-the-art **testing equipment**

• **design portfolio** that can be used during job interviews

• unique knowledge and practical skills that make you competitive on the job market