Kris Gaj

Research and teaching interests:

• reconfigurable computing
• cryptography
• computer arithmetic
• high-level synthesis

Contact:

The Engineering Building, room 3225
kgaj@gmu.edu
Google “Kris Gaj” →

ECE 448 FPGA and ASIC Design with VHDL
TAs

Javad Bahrami
Ph.D. Student
Member of the Cryptographic Engineering Research Group (CERG) since Sep. 2019

Alex Siebold
MSEE Student
Doing a Master’s Thesis with Dr. Nowzari.
BSEE from GMU.
TA for ECE 331/332.
TAs

Billy Kirkendall

MSEE Student.
Concentration in Controls & Robotics
BSEE from GMU.
TA for ECE 301 Digital Electronics.

Shohidul Islam

Ph.D. Student
Doing Ph.D. under Dr. Khasawneh in the area of Computer Architecture Security.
At GMU since Sep. 2019.
Course Hours

Lecture:

Monday, Wednesday
1:30-2:45 PM, Exploratory Hall, room L003

Lab Sessions:

Tuesday (Javad)
9:00-11:40 AM

Wednesday (Alex & Billy)
7:20-10:00 PM

Friday (Javad & Alex)
8:40-11:20 AM

The Nguyen Engineering Bldg., room 3208
General Section Assignment Rules

• You should do your best to attend all lab meetings of the section you are registered for.

• If you have missed a meeting of your section, please attend a meeting of another section, but give preference in access to the lab equipment to the students attending their own lab section.

• All lab assignment demos should be normally done exclusively during the class time of your section.

• Any requests for exceptions to these rules (due to illness, accident, etc.) should be well documented and presented to the TA & the primary instructor for approval.
Lab Access Rules and Behavior Code

Please refer to

ECE Labs website

and in particular to

Access rules & behavior code
Office Hours Rules

You are welcome to attend all office hour sessions! You can direct your questions regarding lab assignments to the TA and the instructor.

Do your best to avoid “chasing” the TAs outside of their office hours! They have other important and often urgent work to do!
Tentative List of Office Hours by the Day of the Week

Monday
- Billy, 11:30-1:30pm, ENGR 3505
- Dr. Gaj, 3:00-4:00pm, ENGR 3225
- Javad, 4:00-5:00pm, ENGR 3208

Tuesday
- Alex, 12:30-2:30pm, ENGR 3208
- Billy, 3:30-5:30pm, ENGR 3203

Wednesday
- Alex, 12:30-2:30pm, ENGR 3505
- Dr. Gaj, 3:00-4:00pm, ENGR 3225

Thursday
- Javad, 1:00-2:00pm, ENGR 3208
Tentative List of Office Hours by the Instructor

Javad
- Monday, 4:00-5:00pm, ENGR 3208
- Thursday, 1:00-2:00pm, ENGR 3208

Alex
- Tuesday, 12:30-2:30pm, ENGR 3208
- Wednesday, 12:30-2:30pm, ENGR 3505

Billy
- Monday, 11:30am-1:30pm, ENGR 3505
- Tuesday, 3:30-5:30pm, ENGR 3203

Shohidul (only regarding quizzes and homework)
- Tuesday, 6:00-8:00pm, ENGR 3204
- Thursday, 6:00-8:00pm, ENGR 3204

Kris Gaj
- Monday, 3:00-4:00pm, ENGR 3225
- Wednesday, 3:00-4:00pm, ENGR 3225
Getting Help Outside of Office Hours

- System for asking questions 24/7
- Answers can be given by students and instructors
- Student answers endorsed (or corrected) by instructors
- Average response time in Spring 2019 = 22 minutes
- You can submit your questions anonymously
- You can ask private questions visible only to the instructors
Electrical Engineering Progression of Core Courses

This is not a suggested schedule. It only illustrates dependencies and shows courses in earliest possible semester.

Not all courses required for the degree are shown.

1) Requires sophomore standing
2) Math 203 can be taken concurrently with ECE 220
3) Requires completion of 45 credits
4) Requires completion of 90 credits applicable to your major

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Prerequisite  Co-Requisite  Co-Requisite +  Semester
Must be taken in  Should be taken con-  Suggested to be  Courses between
sequence         currently but not earlier  taken in sequence  dashed lines can be
dash            dash            dash            taken concurrently

Digital system design technologies coverage in the CpE & EE programs at GMU

Microprocessors

FPGAs

ASICS

ECE 448 FPGA and ASIC Design with VHDL

ECE 445 Computer Organization

ECE 447 Single Chip Microcomputers

ECE 590/ CYSE 499 Computer Architecture Security

ECE 511 Computer Architecture

Advanced Computer Architecture

Real-Time Embedded Systems

ECE 447 Computer Arithmetic

ECE 448 FPGA and ASIC Design with VHDL

ECE 545 Digital System Design with VHDL

ECE 645 Computer Arithmetic

ECE 586 Digital Integrated Circuits

ECE 681 VLSI Design for ASICs

ECE 505 Hardware Security

ECE 615 Software/Hardware Codesign
# Course Web Page

http://ece.gmu.edu/coursewebpages/ECE/ECE448/S20

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<td></td>
<td></td>
<td>Past Lab Exams</td>
</tr>
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Grading criteria

First part of the semester (before the Spring break)

Lab experiments - Part I

16%

Lab exercises – Part I

1.6%

Quizzes & homework: 3%

Midterm exam for the lecture: 10%

Midterm exam for the lab: 15%

Second part of the semester (after the Spring break)

Lab experiments - Part II

24%

Lab exercises – Part II

2.4%

Quizzes & homework: 3%

Final exam

25%
# Tentative Grading Scheme for the Labs

<table>
<thead>
<tr>
<th>Lab 1: Developing VHDL Testbenches</th>
<th>4 points</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lab 2: Combinational &amp; Sequential Logic</td>
<td>4 points</td>
</tr>
<tr>
<td>Lab 3: State Machines. Basic I/O Devices.</td>
<td>8 points</td>
</tr>
<tr>
<td><strong>Total:</strong></td>
<td><strong>16 points</strong></td>
</tr>
<tr>
<td>Lab 4: MicroBlaze – Basic I/O Devices</td>
<td>8 points</td>
</tr>
<tr>
<td>Lab 5: MicroBlaze – Computer Graphics</td>
<td>8 points</td>
</tr>
<tr>
<td>Lab 6: MicroBlaze – Computer Game</td>
<td>8 points</td>
</tr>
<tr>
<td><strong>Total:</strong></td>
<td><strong>24 points</strong></td>
</tr>
</tbody>
</table>
Penalties and Bonus Points

Penalties:

one-week delay: 1/3 of points

i.e., you can earn max. 4 out of 6 points

No submissions or demos will be accepted more than one week after the assignment is due!

Bonus points:

Majority of labs will have opportunities for earning bonus points by doing additional tasks
Flexibility in the Second Part of the Semester

Schedule A:
Lab 4: MicroBlaze – Basic I/O Devices (2 weeks) – 8 points
Lab 5: MicroBlaze – Computer Graphics (2 weeks) – 8 points
Lab 6: MicroBlaze – Computer Game (2 weeks) – 8 points

Total: 24 points

Schedule B:
Lab 4: MicroBlaze – Basic I/O Devices (3 weeks) – 8 points
Lab 5 or Lab 6: MicroBlaze (3 weeks) – 8 points

Total: 16 points
Flexibility in the Second Part of the Semester

Schedule A+

- Intended for students who do very well in the first part of the semester (preferably ≥ 90% of points for Labs 1-3)
- An open-ended project proposed by students, the TAs, or the instructor
- Can be done individually or in groups of two students
- Schedule: Detailed Specification (1 week)
  Milestone 1 (2 weeks)
  Milestone 2 (2 weeks)
  Final Report & Deliverable (1 week)

Total: 30 points
Bonus Points for Class & Piazza Activity

- Based on class exercises during lecture and lab sessions, as well as your answers to other student’s questions on Piazza
- “Small” points earned each week posted on BlackBoard
- Up to 5 “big” bonus points
- Scaled based on the performance of the best student

For example:

<table>
<thead>
<tr>
<th></th>
<th>Small points</th>
<th>Big points</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Alice</td>
<td>40</td>
</tr>
<tr>
<td>2.</td>
<td>Bob</td>
<td>32</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>26.</td>
<td>Zach</td>
<td>8</td>
</tr>
</tbody>
</table>
Exams

• Midterm Exam for the Lecture – 10 points
  Wednesday, February 26

• Midterm Exam for the Lab (hands-on) – 15 points
  Tuesday, March 3
  Wednesday, March 4
  Friday, March 6

• Final Exam – 25 points
  Wednesday, May 6, 1:30-4:15pm
  (first day of the exam session)
Required Textbook

Supplementary Textbook – Basics Refresher

Stephen Brown and Zvonko Vranesic,
*Fundamentals of Digital Logic with VHDL Design*,
Supplementary Textbook – Advanced

ECE 448, FPGA and ASIC Design with VHDL

Topics

VHDL:
- writing testbenches
- writing synthesizable code in VHDL

FPGAs:
- architecture of FPGA devices
- embedded resources (memories, DSP units)
- tools for the computer-aided design with FPGAs
- current FPGA families & future trends
Applications:
- basics of computer arithmetic
- applications from communications, computer vision, cryptography, etc.

Platforms & Interfaces:
- FPGA boards
- I/O modules (VGA controller, serial communication modules)

New Trends:
- microprocessors embedded in FPGAs (MicroBlaze, ARM)
- using high-level programming languages to design hardware

High-level ASIC Design:
- standard cell implementation approach
- logic synthesis tools
- differences between FPGA & standard-cell ASIC design flow
Tasks of the course

Advanced course on digital system design with VHDL
- writing VHDL code for synthesis
- design using division into the datapath & controller
- testbenches
- SW/HW codesign (C/C++ and VHDL)
- high-level synthesis

Comprehensive introduction to FPGAs
- hardware:
  • Xilinx FPGAs
  • FPGAs of other vendors
  • MicroBlaze
- software:
  • Simulators
  • Synthesis tools
  • Implementation tools

Testing equipment
- oscilloscopes
- logic analyzer
VHDL for Specification

VHDL for Simulation

VHDL for Synthesis
Levels of design description

- Algorithmic level
- Register Transfer Level
- Logic (gate) level
- Circuit (transistor) level
- Physical (layout) level

Levels supported by HDL

Level of description most suitable for synthesis
• Use of medium scale-components (adders, multipliers, MUXes, ROMs, RAMs, registers, counters, etc.)
• The designer needs to specify what happens in the circuit in every clock cycle
What is an FPGA?
Modern FPGA

(#Logic resources, #DSP units, #RAM_blocks)

Graphics based on The Design Warrior’s Guide to FPGAs
Devices, Tools, and Flows. ISBN 0750676043
Copyright © 2004 Mentor Graphics Corp. (www.mentor.com)
General structure of an FPGA
Two competing implementation approaches

**ASIC**
Application Specific Integrated Circuit

- designed all the way from behavioral description to **physical layout**
- designs must be sent for expensive and time consuming **fabrication** in semiconductor foundry

**FPGA**
Field Programmable Gate Array

- no physical layout design; design ends with a **bitstream** used to configure a device
- bought **off the shelf** and reconfigured by designers themselves
FPGAs vs. ASICs

**ASICs**
- High performance
- Low power
- Low cost (but only in high volumes)

**FPGAs**
- Off-the-shelf
- Low development costs
- Short time to the market
- Reconfigurability
FPGA Design process (1)

Design and implement a simple unit permitting to speed up encryption with RC5-similar cipher with fixed key set on 8031 microcontroller. Unlike in the experiment 5, this time your unit has to be able to perform an encryption algorithm by itself, executing 32 rounds.

Specification (Lab Assignments)

On-paper hardware design
(Block diagram & ASM chart)

VHDL description (Your Source Files)

Functional simulation

Synthesis

Post-synthesis simulation
FPGA Design process (2)

Implementation

Configuration

Timing simulation

On chip testing
FPGA Boards
Power Supplies

The Basys 3 board can receive power from the Digilent USB-JTAG port (J4) or from a 5V external power supply. Jumper JP3 (near the power switch) determines which source is used. All Basys 3 power supplies can be turned on and off by a single logic-level power switch (SW16). A power-good LED (LD20), driven by the "power good" output of the LTC3633 supply, indicates that the supplies are turned on and operating normally. An overview of the Basys 3 power circuit is shown in Fig. 2.

### Table 1. Basys 3 Callouts and Component Descriptions

<table>
<thead>
<tr>
<th>Callout</th>
<th>Component Description</th>
<th>Callout</th>
<th>Component Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power good LED</td>
<td>9</td>
<td>FPGA configuration reset button</td>
</tr>
<tr>
<td>2</td>
<td>Pmod port(s)</td>
<td>10</td>
<td>Programming mode jumper</td>
</tr>
<tr>
<td>3</td>
<td>Analog signal Pmod port (XADC)</td>
<td>11</td>
<td>USB host connector</td>
</tr>
<tr>
<td>4</td>
<td>Four digit 7-segment display</td>
<td>12</td>
<td>VGA connector</td>
</tr>
<tr>
<td>5</td>
<td>Slide switches (16)</td>
<td>13</td>
<td>Shared UART/ JTAG USB port</td>
</tr>
<tr>
<td>6</td>
<td>LEDs (16)</td>
<td>14</td>
<td>External power connector</td>
</tr>
<tr>
<td>7</td>
<td>Pushbuttons (5)</td>
<td>15</td>
<td>Power Switch</td>
</tr>
<tr>
<td>8</td>
<td>FPGA programming done LED</td>
<td>16</td>
<td>Power Select Jumper</td>
</tr>
</tbody>
</table>
FPGA Tools
Vivado Design Suite

- first version released in Summer 2012
- we will use version 2019.1
- scalable data model, supporting designs with up to 100 million ASIC gate equivalents (GEs)
- Support for VHDL-2008
- Support for High-Level Synthesis
Design Entry Methods

- VHDL
- Verilog, System Verilog
- C, C++, System C
  (for SW/HW codesign and HLS)
- Matlab
- Simulink
Software/Hardware Codesign
FPGA with a Soft-Core Processor

Source: The Zynq Book
Software vs. Hardware Trade-offs

Implement more in Hardware

- Improve Performance
- Improve Energy Efficiency
- Reduce Power Density

Implement more in Software

- Manage Design Complexity
- Reduce Design Cost
- Stick to Design Schedule

Source: A Practical Introduction to Hardware/Software Codesign
High-Level Synthesis

High Level Language
C, C++, System C

Vivado
HLS

Hardware Description Language
VHDL or System Verilog
Additional Simulation Tool

ModelSim®

ModelSim-Intel FPGA Starter Edition

ModelSim:
• Industry standard for simulation
• Significantly faster than Vivado Simulator
• Windows, Linux OS
• Mixed-language support: VHDL, Verilog, System Verilog
• Recommended for advanced users and more complex designs
• To be used primarily as a tool for functional simulation

Features of the Starter Edition:
• Free, no license required
• 10,000 executable line limit
Why ECE 448 is a challenging course?

• need to refresh and strengthen your VHDL skills

• need to learn new tools

• need to perform practical experiments

• time needed to complete experiments
Difficulties
(based on a student survey)

• finding time to do the labs  – 15

• learning VHDL  –  2

• getting used to software  –  1
Why is this course worth taking?

- **VHDL** for synthesis: one of the most sought-after skills
- Knowledge of state-of-the-art tools used in the industry
- Knowledge of the modern FPGA & ASIC technologies
- Knowledge of state-of-the-art testing equipment
- Design portfolio that can be used during job interviews
- Unique knowledge and practical skills that make you competitive in the job market