ECE 545
Midterm Exam 2
Fall 2004

Problem

Function

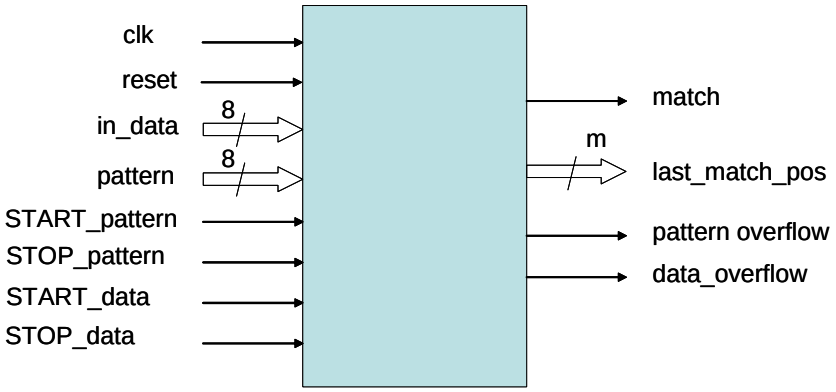
Design and describe using RTL VHDL a circuit capable of processing a stream of up to 2^m data bytes in search of a specific data pattern, of the size of k bytes. The circuit should detect the pattern, and output the position of the given pattern each time it appears in the input data stream.

Optimization

Optimize your circuit for the maximum data throughput. When choosing between two circuits with the same or very similar throughput, give preference to the circuit with the smaller area.

Interface

Assume the following interface to your circuit:



Port	Width	Meaning
clk	1	System clock
reset	1	System reset – clears internal registers
in_data	8	Input data stream
pattern	8	Input for the data pattern
START_pattern	1	Marks the beginning of the pattern
STOP_pattern	1	Marks the end of the pattern
START_data	1	Marks the beginning of the data stream
STOP_data	1	Marks the end of the data stream
last_match_pos	1	Position of the last match (0 if no previous match), counted as a position of the first byte of the matching k-byte data block
match	1	Indicates a match between a pattern and the currently processed k-byte block of the data stream
pattern_overflow	1	size of the pattern exceeds k bytes
data_overflow	1	number of data bytes exceeds 2^m

Verification

Verify your circuit using functional simulation for the case of k=4 and m=8 using a testbench capable of reading input data from a text file in the hexadecimal notation, and writing output data to a text file in the hexadecimal notation.

Synthesis

Synthesize your circuit using Synopsys for the two cases: {k=4, m=8} and {k=16, m=32}, using the 90 nm TCBN90G TSMC library

Based on the synthesis reports, determine for each case:

a. circuit area
b. minimum clock period
c. maximum input data throughput

Suggested design steps

1. Draw a block diagram of the execution unit of your circuit
2. Draw a block diagram of a part of the control unit of your circuit
3. Describe the remaining portion of the control unit using ASM chart
4. Translate ASM chart from actions to values of specific control signals
5. Describe an interface to your circuit in VHDL
6. Translate block diagrams designed in steps 1 and 2 to VHDL
7. Translate the final ASM chart obtained in step 4 to VHDL
8. Write a testbench capable of simulating your circuit
9. Verify the operation of your circuit using functional simulation, introduce corrections in your code if necessary
10. Synthesize and implement your circuit.
11. Determine circuit area, minimum clock period, and worst case execution time based on the implementation reports.

Deliverables *(TO BE SUBMITTED BY WEBCT):*

Handwritten on paper, scanned, and converted into a JPG file, or in the form of a Power Point, MS Word, or a PDF file

1. All block diagrams you have developed
2. All ASM charts you have developed

Electronic version

1. All source codes describing your circuit
2. All testbench files, including input and corresponding output files
3. All Synopsys script files and post-synthesis reports
4. A short text or MS Word file describing circuit area, minimum clock period, and maximum data throughput.
5. Waveforms from the functional simulation.