Tutorial

on

Simulation using Aldec Active-HDL

ver. 2.5

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**Introduction:**

Active-HDL is an integrated environment designed for development of VHDL designs. The core of the system is a VHDL simulator. Along with debugging and design entry tools, it makes up a complete system that allows you to write, debug and simulate VHDL code. Based on the concept of a design, Active-HDL allows you to organize your VHDL resources into a convenient and clear structure.

Students can perform the following tasks:

- Development of VHDL based design,
- Functional simulation of their code,
- Functional simulation of the synthesized code,
- Timing simulation of the hardware implementation.

**Objective:**

This tutorial helps you to

- Create a new design or add .vhd files to your design
- Compile and debug your design
- Perform Simulation

Note: This tutorial does not explain the synthesis or implementation steps.

**Start-up**

1. Start => VLSI Tools => Active-HDL 8.3
a. Select “Create new workspace” and click OK.
b. If you select “open existing workspace”, you can choose any previous workspace that already exists.

2. Select a name and location for the workspace and click ok.
3. Select “Create an Empty Space” and click OK.
4. Choose the block diagram configuration as “Default HDL Language” and default HDL Language as “VHDL”. Select the target technology and click “Next”.

![Property Page dialog box with design language and target technology set to VHDL and Xilinx Virtex-5](image-url)
5. Select a name of the design and click OK.
click “Finish”

6. To the left, the workspace and design in displayed.
You can either add any existing file to the workspace or create a new file using the Tool’s text editor.

7. To add existing files Go to Add New Files => Add Files to Design, and browse the directory containing the source files.
8. To create a VHDL source file, Go to Add New File => New => VHDL Source
Click “Next”.

New Source File Wizard

This wizard will create a source file with initial VHDL code using the design specifications you will enter in the following wizard dialogs.

The generated source file will contain the entity declaration, port declarations and empty architecture body.

☑ Add the generated file to the design

Clear this check box if you do not want to add the file generated by the wizard to the current design.
9. Choose an appropriate name for the “Source File”. Select a name of the “Entity”. For consistency, please pick the same name for the VHDL source file and name of the Entity. Choose a name for the “Architecture”.

![New Source File Wizard - Name](image-url)
10. You can also add Input and Output ports from the dialogue box below by selecting a Name, Port Direction, Array Index and Type. In the end click “Finish”.

![New Source File Wizard - Ports](image)
-- Description:

-- This comment is automatically maintained and may be overwritten.

library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity lab3_demo is
port (  
in1 : in STD_LOGIC;
in2 : in STD_LOGIC;
out1 : out STD_LOGIC  
);
end lab3_demo;

architecture structural of lab3_demo is
begin
  -- enter your statements here --
end structural;
Compile: Once all files are added to the workspace, now you have to “Compile” them to create the simulation model of the described circuit. The compiler checks all the syntax and writes all the necessary information in internal binary format.

11. Right Click the file you want to compile and select “Compile”. You can also combine all source files by clicking “Compile All”.

![Image of Active-HDL interface with Design Browser open and menu options for Compile and other actions]
Simulation: Once you have all the source files compiled, the design can be simulated for functional correctness.

12. From the menu bar, select “Simulation => Initialize Simulation”,

```vhdl
library work;
use work.lab3.library;

entity lab3demo_tb is
  -- Constant CLK_PERIOD : time := 20 ns;
  signal clock : std_logic := '0';
  signal reset : std_logic := '0';
end entity lab3demo_tb;
```
13. Now you have to select the signals you want to monitor, copy them to the simulation window and proceed. For this example, we select all signals of the design and paste them to the simulation window.
14. Click on button to start the simulation, Press if you want to stop the simulation. 
You can also press , if you want the simulation to run for the specified amount of time.