**Homework 1**

**due Thursday, September 14, 4:30pm**

**(submission in the handwritten/printed format in class**
***or***
**in the electronic format using Blackboard)**

**Note: In all of the problems below assume that signed integers use a two's complement representation**

**Problem 1**

A. Show how to implement an inverter using an XOR gate.
B. Show how to implement a conditional inverter using an XOR gate.
   A conditional inverter is defined as follows:
   y=x' if c=1; y=x if c=0 (where x' denotes x complement)

**Problem 2**

Are the following sets of gates complete sets? Are they minimal complete sets?
Justify your answers.

A. {XOR}
B. {XNOR, AND}
C. {XOR, XNOR, OR}

**Problem 3**

Given a 4-bit adder, performing the operation S=X+Y, show how to implement an adder/subtractor, which performs addition when the control input sub=0, and subtraction when sub=1.

**Problem 4**

Explain the difference between

a) Full Adder

b) Half Adder

c) 4-bit unsigned adder

d) 4-bit signed adder

f) 4-bit incrementer

by

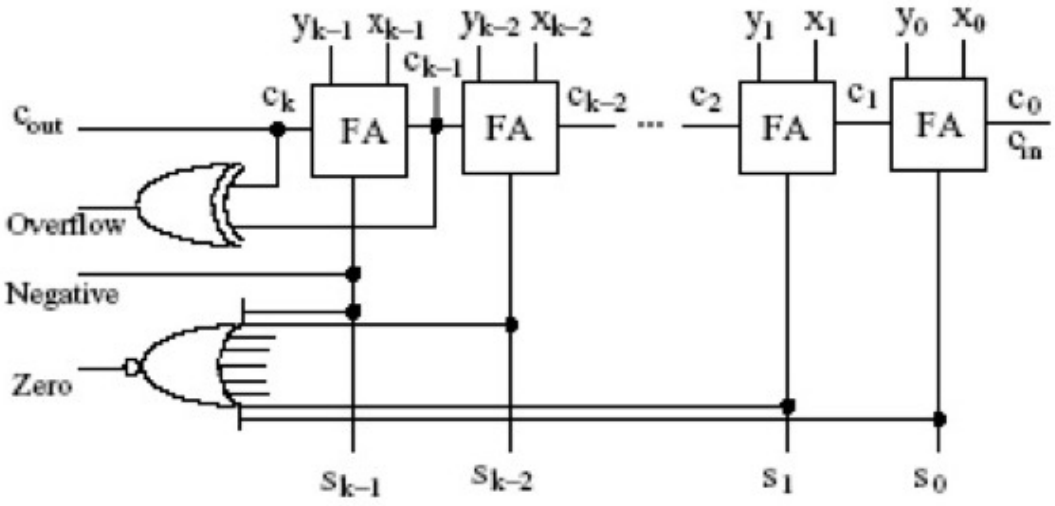
1) defining operations performed by these circuits using arithmetic (not Boolean) equations
2) drawing block diagrams of these circuits using lower-level components.

**Problem 5**

Using the diagram below and your knowledge of the operation of the Full Adder, prove the logical equivalence of the following two equations for the Overflow flag of a *k*-bit adder, performing the operation S=X+Y+$c_{in}$.

$Overflow = c_{k-1} \oplus c_k$

$Overflow = x'_{k-1}y'_{k-1}s_{k-1} + x_{k-1}y_{k-1}s'_{k-1}$




**Problem 6**

Find four examples of a 4-bit integer addition S=X+Y, performed by the circuit from Problem 5 (with k=4 and $c_{in}$=0), for which

a) Carry flag = 0, Overflow flag=0
b) Carry flag = 1, Overflow flag=0
c) Carry flag = 0, Overflow flag=1
d) Carry flag = 1, Overflow flag=1

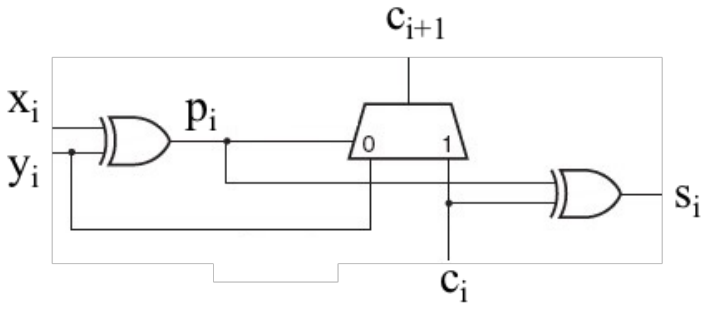
where
Carry flag represents going out of range for unsigned integers,
Overflow flag represents going out of range for signed integers,
X, Y, and S are 4-bit integers (treated as unsigned when the value of the Carry flag is determined, and as Signed when the value of the Overflow flag is determined).

For each addition show values of X, Y, and S

a. in binary representation (e.g., 0110, 1101, etc.)
b. as an unsigned integer (e.g., 6, 13, etc.)
c. as a signed integer (e.g., 6, -3, etc.).

**Problem 7**

Prove that the following circuit performs the same operation as a Full Adder.




**Problem 8**

A. Determine and express in the binary representation the
   a. smallest product of two 4-bit unsigned integers
   b. largest product of two 4-bit unsigned integers
   c. smallest product of two 4-bit signed integers
   d. largest product of two 4-bit signed integers.

B. Prove rigorously, using mathematical derivations, that the product of two *n*-bit signed integers can be always represented using 2*n* bits.

**Problem 9**

Given the equation

$$S = \sum_{i=0}^{m-1} X_i$$

where $X_i$ is a *k*-bit unsigned integer,

A. Determine the maximum value of *S* for *k*=4 and *m*=8.
B. Determine the minimum number of bits required to store *S* for *k*=4 and *m*=8.
C. Determine the maximum value of *S* for *k*=4 and *m*=12.
D. Determine the minimum number of bits required to store *S* for *k*=4 and *m*=12.
E. Prove rigorously, using mathematical derivations, that the minimum number of bits required to store *S* is equal to

$$k + \lceil log_2 m \rceil$$

**Problem 10**

Draw a schematic of the

A. 16-to-1 multiplexer built of the 4-to-1 multiplexers
B. 4-to16 decoder built of the 2-to-4 decoders and a minimum number of logic gates
C. circuit that calculates the maximum of two 4-bit unsigned integers A and B, built of comparators and multiplexers.
D. circuit that calculates the majority function of four variables, x3, x2, x1, x0, built using a ROM. On a separate diagram, show the full contents of the ROM.

**Problem 11**

Show how to implement an address decoder that recognizes the following four ranges of a 16-bit address ADDR, and generates the corresponding enable signals e0, e1, e2, e3, indicating that the address is in the given range:

```
Range 0:   8000-87FF
Range 1:   9000-97FF
Range 2:   A000-A7FF
Range 3:   B000-B7FF
```

All enable signals should be equal to 0, when the address ADDR does not belong to any of the above ranges.

**Problem 12**

1) Show how to implement a variable rotator left, C = A<<<B, rotating the content of an 8-bit input A by the number of positions given by a 3-bit input B, treated as a 3-bit unsigned integer. **Hint:** Use fixed rotators X<<<1, X<<<2, etc., and 2-to-1 multiplexers.
2) How will your answer for question 1) change if B is assumed to be an 8-bit unsigned integer? If it does, please draw a new diagram.
3) Show how to implement a variable shifter left, C = A<<B, shifting the content of an 8-bit input A by the number of positions given by a 3-bit input B, treated as a 3-bit unsigned integer.
4) How will your answer for question 3) change if B is assumed to be an 8-bit unsigned integer? If it does, please draw a new diagram.