Problem 1

(1/3)
* parts of the circuit marked with * do not affect the final result, and thus can be removed from the optimized version of the circuit
Problem 1 - Task 3

Latency = \((1+(k/2))\cdot T_{CLK} + n \cdot T_{CLK}' = (k/2+1+n)\cdot T_{CLK}'\)

\(T_{CLK}' = d_{FF} + d_{XOR} + d_{INV} + d_{MUX}(s\rightarrow y) + d_{XOR} + d_{AND} + d_{FA}(x\rightarrow s) + d_{FA}(\text{cin}\rightarrow s) + d_{MUX2}(x\rightarrow y) + t_{\text{setup}}\)

\(T_{CLK}'' = T_{CLK}' + 2\cdot d_{FA}(\text{cin}\rightarrow cout) + d_{MUX2}(x\rightarrow y)\)

\(n = \text{ceil}(T_{CLK}'') / T_{CLK}'\)