

Final Exam
25 points total

May 11, 2009

Problem 1 (5 points)

1. Draw a detailed block diagram for a 4-bit *signed* Radix-4 Sequential Multiplier with Radix-4 Booth Recoding based on the Shift/Add Algorithm, Right-Shift version, capable of computing $p = a \cdot x + y$, where a , x , and y are all 4-bit signed numbers.
2. Mark the critical path in your circuit.
3. Write a detailed formula for the minimum latency of this multiplier.

Assume that:

- a. you can use only D-flip flops, full adders, half-adders, 2-to-1 multiplexers, inverters, and AND, OR, and XOR gates
- b. the design should be optimized for the minimum product of latency times area
- c. in your diagram you can use connections by name, i.e., two nodes with the same name are connected without drawing a line between them
- d. you do not need to design the corresponding control unit, but you should give name to all control signals required by your design
- e. all outputs from the controller are registered
- f. you should assign names and denote widths for all signals and buses in your design.

Problem 2 (5 points)

1. Show all operands, intermediate values and final results (in the two's complement representation) generated during the *non-restoring signed* division of an 8-bit dividend, z , by a 4-bit divisor, d , for the case of

$$z = -37 \text{ and } d = 5.$$

2. Demonstrate how the same results can be obtained using the concept of *restoring* division. Show all operands, intermediate values and final results for this method.

Problem 3 (5 points)

1. Derive the formulas for the *latencies* (in nanoseconds) and *throughputs* (in operations per seconds) of the following arithmetic circuits *without pipelining*:
 - a. 16-bit Hybrid Brent-Kung/Kogge-Stone Adder
 - b. 8x8-bit radix-2 sequential multiplier based on the Shift/Add Algorithm, Right-Shift version with Carry Save Adder
 - c. 8x8-bit unsigned tree multiplier
 - d. fractional unsigned restoring array divider with a 16-bit dividend and an 8-bit divisor.
2. Which of the listed above circuits can be pipelined?
3. For all circuits that can be pipelined, derive the formulas for *latencies* and *throughputs* of the corresponding circuits after pipelining.

Assume that all circuits are composed of Full Adders, Half-Adders, Modified Half-Adders, 2-to-1 multiplexers, and basic logic gates (NOT, AND, OR, and XOR).

Problem 4 (5 points)

1. Draw a detailed block diagram of a 4x4-bit *pipelined signed Modified Baugh-Wooley* multiplier.
2. Calculate the area, throughput, and latency of a $k \times k$ multiplier of the same type, assuming that the circuit is composed of 2-input NAND gates only.

Assume that

- your circuit does not include any surrounding shift registers or registers
- all inputs, including control inputs, are registered (outside of your circuit)
- D flip-flop is composed of 6 2-input NAND gates, has a clock-to-output delay of 2 NAND gate delays, and the setup time of 1 NAND gate delay
- unit of delay is a delay of a 2-input NAND gate
- unit of area is an area of a 2-input NAND gate

Perform the following tasks:

- a. Draw a block diagram of this circuit using medium level components, such as multiplexers, half-adders, modified half-adders, full-adders, flip-flops, etc.
- b. Draw a detailed schematic of all combinational components of your circuit (no schematic required for a flip-flop).
- c. Determine areas and delays of all combinational components of your circuit.
- d. Determine general formulae for the Clock Period, Latency, Throughput, and Area of this circuit as a function of k .

Problem 5 (5 points)

Squaring of m -bit operands, $y=i^2$, can be implemented using a look-up table defined as follows:

$$\text{TABLE}[i] = i^2 \quad \text{for } i = 0 \text{ to } 2^m - 1.$$

1. Determine the largest value of m , for which such a table can be built using a single Block RAM of Spartan 3 FPGAs.

Multiplication of two k -bit numbers a and x can be computed using the following dependence:

$$p = a*x = ((a+x)^2 - (a-x)^2) / 4$$

2. Draw a block diagram of a circuit capable of performing *unsigned* multiplication using this dependence and the method for squaring defined above.

Follow the following requirements:

- The circuit should operate correctly for an arbitrary dependence between a and x , and an arbitrary value of k .
- Use the minimum number of adders and Block RAMs.
- Assign names and denote widths for all signals and buses in your design.
- Clearly specify the sizes of all memories you use.

Hint: A Block RAM in a Spartan 3 FPGA can be configured as dual port RAM of the size of up to 18 kbits, with different aspect ratios, i.e., different widths of the address bus vs. data bus leading to the same capacity.

Bonus Problem (2 points):

How would you modify your circuit from solution to Problem 5 in order to implement *signed* multiplication of two k -bit numbers?