

Final Exam
25 points total

May 8-9, 2010

Problem 1 (5 points)

1. Draw a detailed block diagram for a 4-bit unsigned Radix-4 Sequential Multiplier with Radix-4 Booth Recoding based on the Shift/Add Algorithm, Right-Shift version, with Carry Save Adder, capable of computing $p = a \cdot x + y$, where a , x , and y are all 4-bit unsigned numbers.
2. Mark the critical path in your circuit.
3. Write a detailed formula for the minimum latency of this multiplier.

Assume that:

- a. you can use only D-flip flops, full adders, half-adders, 2-to-1 multiplexers, inverters, and AND, OR, and XOR gates
- b. the design should be optimized for the minimum product of latency times area
- c. in your diagram you can use connections by name, i.e., two nodes with the same name are connected without drawing a line between them
- d. you do not need to design the corresponding control unit, but you should give name to all control signals required by your design
- e. all outputs from the controller are registered
- f. you should assign names and denote widths for all signals and buses in your design.

Problem 2 (5 points)

Show all operands, intermediate values, and the final results (in binary notation) generated during the execution of the following multiplication in the circuit from Problem 1 (all operands given in decimal notation):

$$a = 11$$

$$x = 14$$

$$y = 12.$$

Problem 3 (5 points)

Design a circuit implementing rounding scheme called “Round to nearest, ties to even (rtne)”, used as a default rounding scheme in the ANSI/IEEE 754 floating point representation standard. Assume that the input is a signed number in the two’s complement representation composed of 8 bits in the integer part and 4 bits in the fractional part. The output is a 8 bit integer and a carry out bit.

Assume that

- your circuit is purely combinational, optimized for minimum area, and composed of internal structures of Spartan 3 FPGAs, namely LUTs and fast carry chain logic (LUT + 2-to-1 MUX + XOR gate) used to speed up addition
- the delay of a LUT is 1 ns, the delay of a fast-carry-chain MUX is 0.1 ns from carry in to carry out, and 0.25 ns from the select signal to carry out, and the delay of a fast-carry-chain XOR gate is 0.25 ns
- delays of interconnects should be neglected in your computations.

Perform the following tasks:

- a. Draw a block diagram of this circuit using medium and low level components, such as multiplexers, half-adders, modified half-adders, full-adders, gates, etc.
- b. Draw a detailed schematic of all major components of your circuit using internal structures of Spartan 3 FPGAs
- c. Determine formulae for the Latency (in ns) and Area (in LUTs) of the entire circuit.

Problem 4 (5 points)

Implement in VHDL one of the following two circuits:

1. $k \times k$ -bit *pipelined signed Modified Baugh-Wooley* multiplier
- or*
2. *sequential Radix-2 restoring unsigned integer divider*, with the dividend size $2k$ bits and the divisor size k bits.

Submit:

1. synthesizable source code
2. testbench
3. waveforms demonstrating the correct operation of your circuit
4. results of synthesis and implementation for $k=16$, $k=32$, and $k=64$
5. short report showing your calculations of Latency (in ns) and Throughput (in operations per second) for the implemented circuit.

Problem 5 (5 points)

Squaring of m -bit operands, $y=i^2$, can be implemented using a look-up table defined as follows:

$$\text{TABLE}[i] = i^2 \quad \text{for } i = 0 \text{ to } 2^m - 1.$$

1. Determine the largest value of m , for which such a table can be built using a single Block RAM of Spartan 3 FPGAs.

Multiplication of two k -bit numbers a and x can be computed using the following dependence:

$$p = a*x = ((a+x)^2 - (a-x)^2) / 4$$

2. Draw a block diagram of a circuit capable of performing *unsigned* multiplication using this dependence and the method for squaring defined above.

Follow the following requirements:

- The circuit should operate correctly for an arbitrary dependence between a and x , and an arbitrary value of k .
- Use the minimum number of adders and Block RAMs.
- Assign names and denote widths for all signals and buses in your design.
- Clearly specify the sizes of all memories you use.

Hint: A Block RAM in a Spartan 3 FPGA can be configured as dual port RAM of the size of up to 18 kbits, with different aspect ratios, i.e., different widths of the address bus vs. data bus leading to the same capacity.

Bonus Problem (2 points):

How would you modify your circuit from solution to Problem 5 in order to implement *signed* multiplication of two k -bit numbers?