

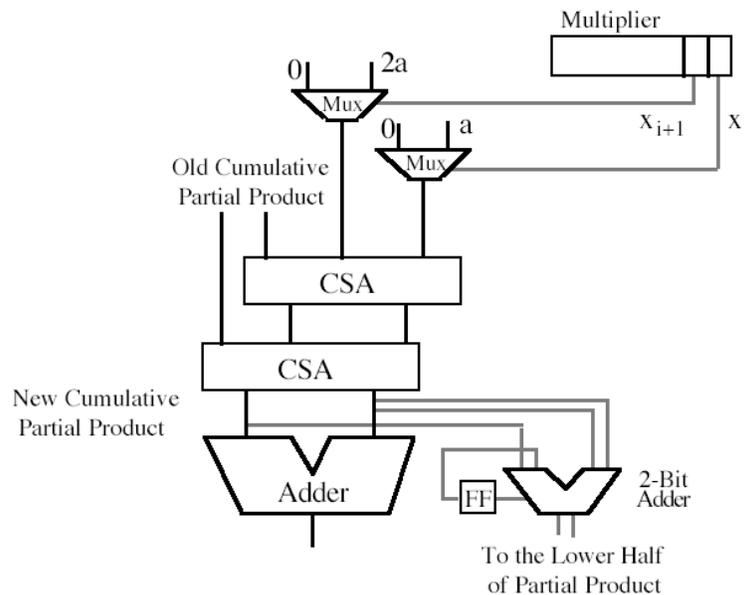
Final Exam 30 points + 5 bonus points

May 8, 2013

Problem 1 (10 points)

Perform the given below tasks for the unsigned Radix-4 shift/add sequential multiplier with right shift, two carry-save adders, and the upper half of the cumulative partial product kept in the carry-save form, capable of computing $p = a \cdot x + y$, where a , x , and y are all k -bit unsigned numbers.

A part of this multiplier is shown conceptually below:



1. Draw a detailed block diagram, based on D flip-flops, multiplexers (with each data input of the size of 1 bit), Full Adders, Half-Adders, and logic gates, for $k=4$.
2. Draw a generalized block diagram, based on registers (of arbitrary size), multiplexers (with arbitrary size of data inputs), adders (with arbitrary size of operands), bit-by-word logic operators (e.g., b AND a , where b is a bit, and a is a k -bit word), and logic gates, for arbitrary value of k .
3. Mark the critical path on both block diagrams.
4. Derive the formulas for the following performance metrics of the $k \times k$ bit multiplier (assuming k is even):
 - a. Minimum clock period, as a function of the delays and timing parameters of basic logic components (e.g., d_{FF} , d_{AND2} , t_{setup}), and the parameter k
 - b. Minimum latency
 - c. Maximum throughput (in multiplications per second).

5. In a simple table, provide values of the control signals used by your circuit during all clock cycles necessary for initializing the circuit and computing $p = a \cdot x + y$, for $k=4$.

Assume that:

- in your diagram you can use connections by name, i.e., two nodes with the same name are connected without drawing a line between them
- you do not need to design the corresponding control unit, but you should give name to all control signals required by your design
- all outputs from the controller are registered
- you should assign names and denote widths for all signals and buses in your design.

Problem 2 (6 points)

Show all operands, intermediate values, and the final results (in binary notation) generated during the execution of the following multiplication in the circuit from Problem 1 (all operands given in the decimal notation):

$$k = 4$$

$$a = 10$$

$$x = 14$$

$$y = 13.$$

Problem 3 (6 points)

Show all operands, intermediate values, and the final results (in decimal and binary notation) generated during the execution of the following division by the non-restoring signed integer divider, described by the given below pseudocode.

$$k=4$$

$$z = -45$$

$$d = 7.$$

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s(0) = z
for j = 1 to k
  if sign(s(j-1)) == sign(d)
    qk-j = 1
    s(j) = 2 s(j-1) - 2k d = 2 s(j-1) - qk-j (2k d)
  else
    qk-j = -1
    s(j) = 2 s(j-1) + 2k d = 2 s(j-1) - qk-j (2k d)

q = BSD_2' s_comp_conversion(q)
Correction_step

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Problem 4 (8 points)

Design a 4x4 **unsigned tree squarer mod 13**, i.e., the **combinational** circuit that performs operation

$$s = a^2 \bmod 13$$

for a 4-bit input a .

As intermediate steps in your design, please provide:

- table of partial products,
- dot diagram, and
- detailed block diagram.

Assume that you can use the following components in your block diagram: Full Adders, Half-Adders, Modified Half-Adders, 2-to-1 multiplexers, and basic logic gates (NOT, AND, OR, and XOR).

Your optimization target should be the minimum product of latency times area.

Bonus Problem 5 (5 bonus points)

Write a **truth table** for the Radix-8 Booth Recoding Logic, with inputs (x_{i+2} , x_{i+1} , x_i , and x_{i-1}), and outputs (neg, two, four, non0).

Implement this circuit using NOT, AND, OR, and XOR gates with up to 4 inputs.

Show how the outputs from this circuit can be used to generate multiples:

$-4a$, $-2a$, $-a$, 0 , a , $2a$, $4a$.