

ECE 645: Spring 2007
Exam 2
Saturday, Sunday – May 5-6, 2007

Develop and debug synthesizable Register Transfer Level (RTL) VHDL code for **one** of the following two arithmetic units:

- A. k-bit unsigned radix-4 sequential multiplier with Booth's recoding
- B. k-bit unsigned radix-2 multiplier with the upper half of the partial product stored in the carry-save form, shown in Parhami in Fig. 10.8.

Please perform the following tasks:

1. Draw a detailed schematic of your circuit for $k=4$.
2. Draw an ASM chart or state diagram describing the behavior of the control unit of your circuit for $k=4$.
3. Check the functionality of your VHDL code for $k=4$ using at least three different test vectors in each case.
4. Set the target FPGA device to the smallest Spartan 3 FPGA capable of holding your circuit for $k=64$. Synthesize your codes for $k=4$ and $k=64$ using Synplify Pro, and implement them using Xilinx ISE. Perform the timing simulation of your circuit for $k=4$ using the same test vectors you used for the functional simulation. Check thoroughly all implementation reports.
5. For both versions of your circuit (with $k=4$ and $k=64$), determine their minimum latency and the number of CLB slices required for their implementation.

Please submit the following deliverables:

1. block diagram of your circuit for $k=4$
2. ASM chart or state diagram describing the control unit of your circuit for $k=4$
3. source codes of the
 - main circuit
 - test circuit (if any)
 - testbench
4. waveforms demonstrating the correct timing simulation of your circuits at their maximum clock frequency for three different test vectors
5. short report containing at least the description of the
 - circuit interface
 - test vectors
 - minimum number of CLB slices
 - minimum latency.