

**Midterm Exam 1**  
**15 points total**

**March 23, 2009**

**Part I**  
**Analytical Problems**

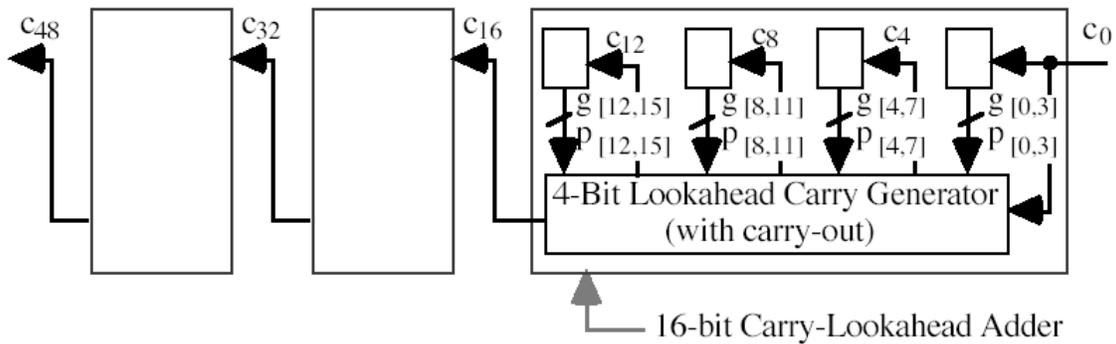
1. **(1.5 points)**
  - A. Represent the following negative number, -97.8125, using
    - a. signed magnitude representation,
    - b. one's complement representation,
    - c. two's complement representation,
    - d. biased representation with the bias  $B=2^7$ ,all with 8 bits in the integer part and 4 bits in the fractional part.
  - B. Extend the obtained representations to the equivalent representations with 12 bits in the integer part and 8 bits in the fractional part.
  
2. **(1.5 points)** Compute value of the expression  $C='3' \cdot A^2$  in the Galois Field  $GF(2^4)$  for  $A='6'$ . Assume that an irreducible polynomial  $P(x)$  is equal to  $P(x)=x^4+x+1$ .
  
3. **(1.5 points)** Determine all bits of the ANSI/IEEE standard single-precision representation of the following numbers:
  - a.  $(-5/0) * 0$
  - b.  $-0.0FEDCBA9_{16} \times 16^{+33}$
  - c.  $-12.34567654321_8 \times 8^{-43}$
  - d.  $1111.1100110010101010_2 \times 2^{-130}$

**Hint:** Use the default IEEE rounding scheme whenever appropriate.

4. (1.5 points) Arrange the listed below signals in the order they are generated within the 48-bit Hybrid Ripple-Carry/Carry-Lookahead Adder shown in the figure below. For each signal calculate the time when this signal becomes stable for arbitrary values of inputs, assuming that all inputs change at the time 0.

Assume that

- The adder is built out of AND, OR, and XOR gates with up to 5 inputs, and the delays of all these gates are equal.
- 4-bit Lookahead Carry Generators at the Level 2 produce carry out, at the same time as remaining carry bits (i.e.,  $c_4$ ,  $c_8$ ,  $c_{12}$ , and  $c_{16}$  all appear at the same time for the 4-bit Lookahead Carry Generator shown in the figure).



- A.  $g_{[20, 23]}$   
 B.  $s_{15}$   
 C.  $c_{28}$   
 D.  $c_{32}$   
 E.  $s_{35}$

**Part II**  
**Design Problems**  
**(3 points for each problem)**

1. Derive a general formula for the ratio of the delays of a k-bit Hybrid Brent-Kung/Kogge-Stone Adder and a k-bit Carry-Lookahead Adder. Compute the value of this ratio for  $k=16, 64,$  and  $256$ .

Assume that:

- inputs to the adders are  $x_i, y_i, cin=c_0,$  and outputs are  $s_i, cout=c_k$
- $k$  is of the form  $k=2^m$
- adder is composed of inverters and AND, OR, and XOR gates with up to 4 inputs
- delays are the same for all gates
- unit of delay is a delay of a single gate.

2. Design a k-bit digit-serial decrementer, with the digit size d, optimized for minimum area and composed of 2-input NAND gates only.

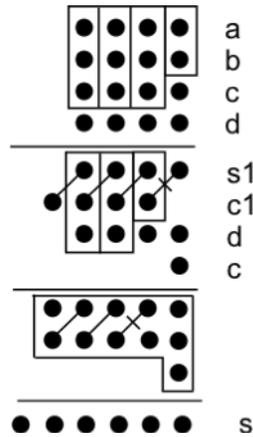
Assume that

- your circuit does not include any surrounding shift registers or registers
- control signals, such as START, are provided externally
- all inputs, including control inputs, are registered (outside of your circuit)
- D flip-flop is composed of 6 2-input NAND gates, has a clock-to-output delay of 2 NAND gate delays, and the setup time of 1 NAND gate delay
- unit of delay is a delay of a 2-input NAND gate
- unit of area is an area of a 2-input NAND gate

Perform the following tasks:

- a. Draw a block diagram of this circuit using medium level components, such as multiplexers, half-adders, modified half-adders, full-adders, flip-flops, etc.
- b. Draw a detailed schematic of all combinational components of your circuit (no schematic required for a flip-flop).
- c. Determine areas and delays of all combinational components of your circuit.
- d. Determine general formulae for the Clock Period, Latency, and Area of your decrementer as a function of  $k$  and  $d$ .

3. Translate the following dot diagram into the corresponding digital circuit.



Perform the following tasks:

- a. Draw a block diagram of this circuit using medium level components, such as full-adders and half-adders.
- b. Clearly mark names and indices of all signals in your schematic, using notation such as  $a_0$ ,  $b_1$ ,  $s_{10}$ ,  $c_{13}$ , etc.
- c. Determine the minimum number of 4-input Look-Up Tables (LUTs) necessary to implement this circuit using Xilinx Spartan 3 devices, assuming that
  - Full adders within Carry Save Adders are implemented using LUTs only
  - Full adders within a Carry Propagate Adder and half-adders within both types of adders are implemented using fast carry chain logic (LUT + 2-to-1 MUX + XOR gate)
- d. **(bonus 1 pt)** determine the critical path and delay of this circuit assuming that
  - the delay of a LUT is 1 ns, the delay of a fast-carry-chain MUX is 0.1 ns from carry in to carry out, and 0.25 ns from the select signal to carry out, and the delay of a fast-carry-chain XOR gate is 0.25 ns
  - delays of interconnects should be neglected in your computations.