ECE 645
Spring 2014

Homework 2

due Saturday, February 15, 11:59 PM

Problem 1

In the Answer Sheets 1, 2, and 3, fill in yellow boxes, representing values of inputs, intermediate signals, and outputs of the respective adders.

For Part A of each diagram, please assume:

```
X = 1001 1100 1010 0011
Y = 0111 0101 1011 1110
c0 =                  1
```

For Part B of each diagram, please assume:

```
X = 1011 1011 0010 0011
Y = 0100 0100 1101 1110
c0 =                  0
```

Verify your calculations of the carry bits and the sum bits by performing each operation using a 16-bit Ripple-Carry Adder.

Problem 2

Arrange the listed below signals (A-J) in the order they are generated within

1. 64-bit Carry Look-Ahead Adder
2. 64-bit Two-level Carry Select Adder
3. 64-bit Hybrid Carry-Lookahead/Carry-Select Adder (discussed in class).

For each signal calculate the exact time when this signal becomes stable for arbitrary values of inputs, assuming that all inputs to the adder (i.e., X, Y, and cin) change at the time 0.

Assume that the adders are built out of inverters and AND, OR, and XOR gates with up to 4 inputs, and the delays of all these gates are equal to one gate delay, i.e.,

$$d_{ANDn} = d_{XORn} = d_{ORn} = d_{NOT} = 1 \qquad \text{for } n=2..4.$$

Perform the required delay calculations separately for each of the aforementioned three adders.

Assume that each adder has a carry in input, and the carry out and overflow outputs.

Signals of interest are:

A. c_{32}

B. c_{50}

C. c_{8}

D. c_{18}

E. cout = c_{64}

F. overflow V

G. s_{48}

H. s_{60}

I. s_{55}

J. s_{15}

In case an intermediate carry signal has two possible values (and a single value is not computed), calculate the delay necessary to determine both of these values.