ECE 645
Spring 2014

Homework 3

due Wednesday, February 26, 4:30 PM

Problem 1

A. In the Answer Sheet 1, fill in yellow boxes, representing values of intermediate signals and outputs of an upper section of the conditional sum adder, processing bits from 4 to 7.

For Part A of the diagram, please assume:

```
X = 1010 0011
Y = 0011 1010
c0 =         1
```

For Part B of the diagram, please assume:

```
X = 1011 1011
Y = 0101 0101
c0 =         0
```

Verify your calculations of the carry bits and the sum bits by performing each operation using an 8-bit Ripple-Carry Adder.

B. In the Answer Sheet 2, fill in yellow boxes, representing values of intermediate signals and outputs of the Brent-Kung Parallel Prefix Network Adder.

For Part A of the diagram, please assume:

```
X = 1010 0011
Y = 0011 1010
c0 =         1
```

For Part B of the diagram, please assume:

```
X = 1011 1011
Y = 0101 0101
c0 =         0
```

Verify your calculations of the carry bits and the sum bits by performing each operation using an 8-bit Ripple-Carry Adder.

C. In the Answer Sheet 3, fill in yellow boxes, representing values of intermediate signals and outputs of the Hybrid Brent-Kung/Kogge-Stone Parallel Prefix Network. Please note that the diagram shows only the Parallel Prefix Network, and the pre-calculations necessary to calculate (g, p) pairs, as well as post-calculations necessary to calculate carry and sum bits are omitted.

For Part A of the diagram, please assume:

```
X = 1001 1100 1010 0011
Y = 0111 0101 1011 1110
c0 =                  1
```

For Part B of the diagram, please assume:

```
X = 1011 1011 0010 0011
Y = 0100 0100 1101 1110
c0 =                  0
```

Complete your calculations of carry bits and sum bits for both cases, and verify that these calculations return the same results as a 16-bit Ripple-Carry Adder.

Problem 2

Draw a full block diagram of the pipelined 8-bit Hybrid Brent-Kung/Kogge-Stone Parallel Prefix Network Adder.

Derive formulas for the throughput (in additions per unit of a delay), latency, and area of this adder.

Assume that

- All inputs are registered (outside of your circuit).
- The number of pipeline stages has been chosen to optimize throughput.
- Your circuit is composed of D flip-flops, AND gates, OR gates, XOR gates, and inverters.
- Delays of all gates are independent of the number of inputs, and are equal to the delay of an inverter. Thus, you can assume that the delay of each gate and inverter is equal to 1.
- Area of each gate is proportional to the number of inputs. For example, area of a 2-input gate is equal to the area of 2 inverters. Assume that the area of an inverter is equal to 1, area of a 2-input gate is equal to 2, etc.
- Area of a D flip-flop is equal to 12, its clock-to-output delay is equal to 2, and its setup time is equal to 1.

Bonus: Generalize your formulas for the case of a k-bit adder of the same type.