Kris Gaj

Research and teaching interests:

- cryptography
- FPGA design and verification
- software/hardware codesign
- computer arithmetic

Contact:

Engineering Bldg., room 3225
kgaj@gmu.edu

Office hours:  Monday, 3:00-4:00 PM,
              Wednesday, 3:00-4:00 PM,
              Thursday, 6:00-7:00 PM,
and by appointment
Malik Umar Sharif

Research and teaching interests:
• software/hardware codesign
• FPGA design and verification
• Microcontroller system design
• CAD tools

Contact:
Engineering Bldg., room 3231
malik.umar.sharif@gmail.com

Office hours:  Monday, 12:00-1:00 PM, ENGR 3204
               Wednesday, 4:00-5:00 PM, ENGR 3204
               Thursday, 5:00-7:00 PM, ENGR 3231
               and by appointment
Getting Help Outside of Office Hours

- System for asking questions 24/7
- Answers can be given by students and instructors
- Student answers endorsed (or corrected) by instructors
- Average response time in ECE 545 = 1.5 hour
- You can submit your questions anonymously
- You can ask private questions visible only to the instructors
A few words about You

- 9 MS CpE students
- 4 MS EE students
- 2 PhD ECE students
MICROPROCESSOR AND EMBEDDED SYSTEMS

1. ECE 510 Real-Time Concepts
   – P. Pachowicz, project, design of real-time systems

2. ECE 511 Microprocessors
   – J.P. Kaps, project, system based on MSP430 microcontroller

3. ECE 611 Advanced Microprocessors
   – H. Homayoun, project, computer architecture simulation tools

4. ECE 612 Real-Time Embedded System
   – C. Sabzevari, project, programming distributed real-time systems

5. ECE 641 Computer System Architecture
   – H. Homayoun, project, computer architecture simulation tools

6. ECE 699-001 Software/Hardware Codesign
   – K. Gaj, homework, SoC design with VHDL and C

7. ECE 699-003 Heterogeneous Architectures and Green Computing
   – H. Homayoun, project, computer architecture simulation tools
DIGITAL SYSTEMS DESIGN

1. ECE 545 Digital System Design with VHDL
   – K. Gaj, project, FPGA design with VHDL,

2. ECE 645 Computer Arithmetic
   – K. Gaj, project, FPGA design with VHDL or Verilog

3. ECE 681 VLSI Design for ASICs
   – H. Homayoun, project/lab, front-end and back-end ASIC design with Synopsys tools

4. ECE 586 Digital Integrated Circuits
   – D. Ioannou, R. Mulpuri, homework

5a. ECE 682 VLSI Test Concepts
    – T. Storey, homework
5b. ECE 699 Digital Signals Processing Hardware Architectures
    – A. Cohen, project, FPGA design with VHDL and Matlab/Simulink

6. ECE 699 Software/Hardware Codesign
   – K. Gaj, homework, SoC design with VHDL and C
Prerequisites

- ECE 511 Microprocessors
- ECE 545 Digital System Design with VHDL

Useful Knowledge

- Basics of computer organization
- High level programming language (preferably C)
- RTL design with VHDL
- FPGA devices and tools
Software/Hardware Codesign

Lecture

- Midterm exam (in class) 20%
- Final Exam (in class) 30%

Exercises

- Class Exercises 5%
- Homework Exercises* 45%

* up to 6 biweekly assignments; per individual requests these assignments may be replaced by a single project proposed by a given student or a group of two students
Bonus Points for Class Activity

• Based on answers provided during the lecture and on Piazza
• “Small” points earned each week posted on BlackBoard
• Up to 5 “big” bonus points
• Scaled based on the performance of the best student

For example:

<table>
<thead>
<tr>
<th></th>
<th>Small points</th>
<th>Big points</th>
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<tr>
<td>1. Alice</td>
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<td>12. Charlie</td>
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Literature (1)

Required Textbooks:

L.H. Crockett, R.A. Elliot, M.A. Enderwitz, and R.W. Stewart, University of Strathclyde, Glasgow, UK

- *The Zynq Book*: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC
- *The Zynq Book Tutorials*

PDF copies available for free at http://www.zynqbook.com
Supplementary Textbooks:

available for free for GMU students at Springer Link, http://link.springer.com.mutex.gmu.edu

Literature (3)

C & VHDL Resources:


Other Resources

- Video Tutorials
- Tutorials
- Reference Manuals
- User Guides
- Journals
- On-line C Resources
- On-line VHDL Resources
Exams

Midterm Exam – 2 hrs 40 minutes, in class

Final Exam – 2 hrs 45 minutes, in class comprehensive

Tentative days of the exams:

Midterm Exam: Thursday, March 26, 7:20-10:00 PM
Final Exam: Wednesday, May 7, 7:30-10:15 PM
Homework Exercises (1)

- based on the **Digilent ZYBO Zynq-7000 Development Board**
  (distributed for free at the beginning of the semester, and collected at the end of the semester)

- involve **Xilinx Vivado Design Suite**
  (to be installed on your own machines, or used in the lab)

- can be **done individually or in a group of two students**
  (group homework assignments will involve a larger number of tasks and/or more time-consuming tasks)
Homework Exercises (2)

- Up to **6 assignments**

- **Deliverables**, typically due on Thursday @ 5:00 PM, to be submitted on Blackboard

- The corresponding **demo** on Thursday, 5:00-7:00 PM, or after the class

- No deliverables *or* no demo = **one-week late submission**, penalized by 33% of the maximum score

- No submissions accepted more than one week after the deadline

- **Honor code** strictly enforced
Installation of Xilinx Vivado Suite