ECE 699 Software/Hardware Codesign
Final Exam
Spring 2015

First Name: ……..
Last Name: ……..

Part 1: Concepts

1. Explain the primary differences between distributed memory and BRAM in Xilinx Series 7 FPGAs and Zynq

2. List the products of Altera and Microsemi directly competing with Zynq

3. List 3 primary metrics optimized by the Vivado's Analytical Placer

4. Explain the difference between static and dynamic profiling

5. What are the advantages and disadvantages of increasing sampling frequency during profiling?

6. What is a significance of bin size in profiling?

7. What are the advantages of using scatter-gather DMA over simple DMA?

8. Which Xilinx IP core can be utilized to comprehensively test the operation of a user core with AXI interface, using functional simulation (i.e., without the need of running the software/hardware system on the board)?

9. What is a significance of invalidating cache for buffer, and when and under what circumstances this operation should be performed?

10. Which of the following interfaces between PS and PL are particularly suitable for the high-throughput transfer of data between DRAM and a hardware accelerator located in PL? Why?
    a. S_AXI_GP
    b. M_AXI_GP
    c. S_AXI_ACP, or
    d. S_AXI_HP?

11. List at least 3 C-based languages for high-level synthesis, other than C/C++/SystemC

12. Explain the major difference between SystemC 1.0 and SystemC 2.0

13. List at least 3 reconfigurable supercomputers developed in the period 2000-2010

14. List at least 3 major disadvantages of reconfigurable supercomputers compared to traditional supercomputers

15. What was the name of the program that was later converted to Vivado HLS? What was the name of the company that developed that program, and was acquired by Xilinx in 2011?

16. Give the name of at least one academic open-source HLS tool and the name of the university where this tool was developed? What are the major limitations of this tool?

17. Explain the meaning of scheduling and binding in Vivado HLS

18. Give the names of types representing a 24-bit integer in

    C:

    C++:

    SystemC:

19. Describe at least 3 quantization modes of the C++ fixed-point data types

20. What keyword needs to be added in front of the following array declaration to move its initialization from the function execution to the bitstream load.

……. int coeff[8]={-2, 8, -4, 10, 14, 10, -4, 8, -2};

21. What C function infers burst mode?

22. List 3 features of a perfect loop? What is a difference between a semi-perfect loop and a perfect loop?

23. What are the two most important features of the default implementation of a loop after HLS?

24. Explain the meaning of Initiation Interval

25. What is a role and significance of the following directives of Vivado HLS

```
set_directive_allocation –limit 1 –type function foo_top foo
set_directive_inline dummy1
set_directive_inline dummy2
```

for the code

```
void dummy1() {
        foo()
}
void dummy2() {
        foo()
}
void foo_top() {
         dummy1(…)
         dummy2(…)
}
```

26. Explain the role and significance of all pragmas in the following code

```
void mm_parallel_dot_product(int in_a[A_ROWS][A_COLS],
                             int in_b[A_COLS][B_COLS],
                             int out_c[A_ROWS][B_COLS])

#pragma HLS ARRAY_PARTITION DIM=2 VARIABLE=in_a complete
#pragma HLS ARRAY_PARTITION DIM=1 VARIABLE=in_b complete

int sum_mult;
a_row_loop: for (int i = 0; i < A_ROWS; i++) {
   b_col_loop: for (int j = 0; j < B_COLS; j++) {
     #pragma HLS pipeline
                 sum_mult = 0;
                 a_col_loop: for (int k = 0; k < A_COLS; k++) {
                 sum_mult += in_a[i][k] * in_b[k][j];
      }
      out_c[i][j] = sum_mult;
    }
  }
}
```

27. List at least 5 advantages of developing and/or running software under Linux vs. bare metal on Zynq

28. List 2 major disadvantages of using Linux vs. bare metal on Zynq

29. List at least 3 possible boot sources for Linux on Zynq

30. What is a function of device tree in Linux on Zynq?