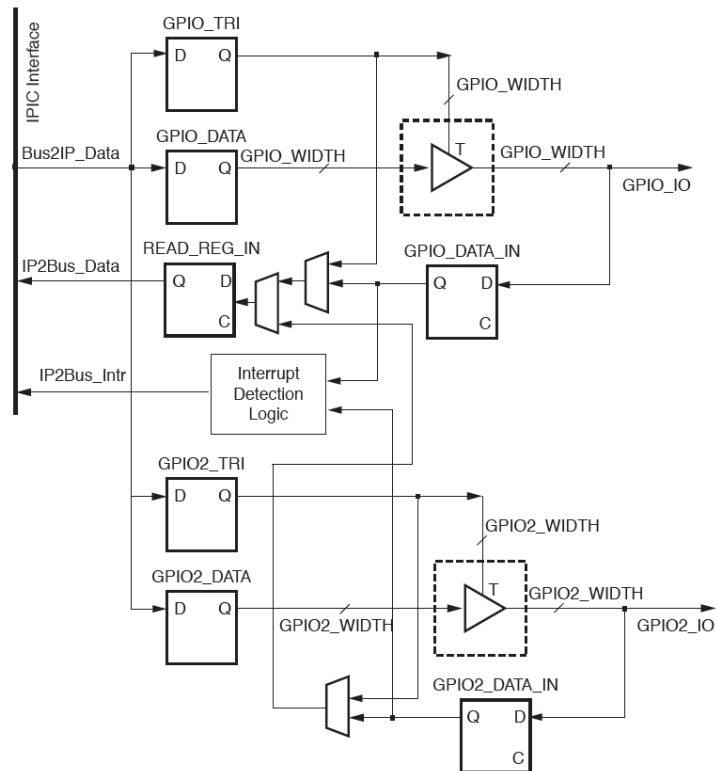
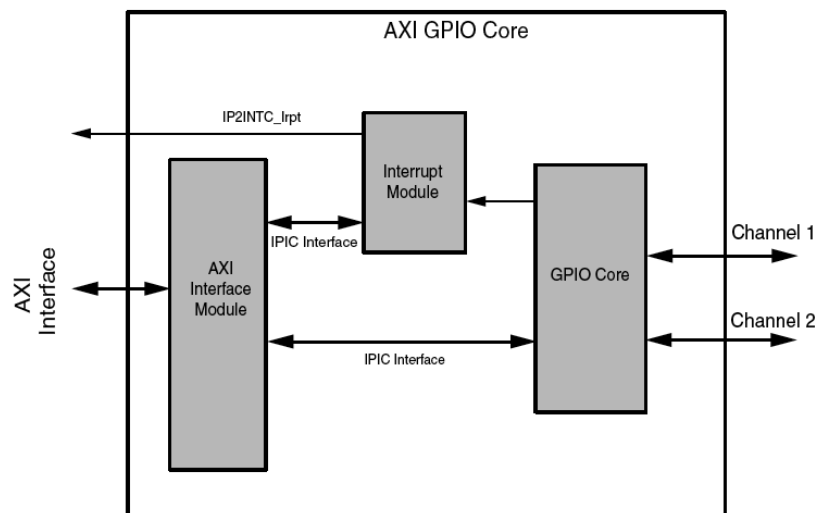
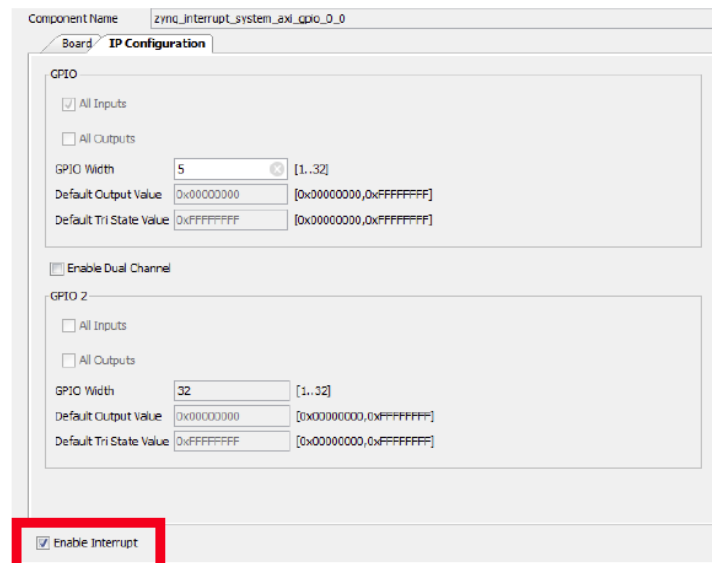


5. List 3 primary metrics optimized by the Vivado's Analytical Placer.

6. Explain the meaning of the dashed rectangles in the block diagram of the GPIO core shown below.



- Explain the effect of unmarking the Enable Interrupt option in the Vivado GUI window shown below on the block diagram of AXI GPIO shown next.



- How many different types of interrupts can be generated by the AXI GPIO configured as shown in Question 7?

9. Which of the following PS-PL interfaces is used for communication between the ARM processors and AXI GPIOs in Zynq?
 - a. S_AXI_GP
 - b. M_AXI_GP
 - c. S_AXI_ACP, or
 - d. S_AXI_HP?

10. List at least 3 possible uses of the Generate Mode of AXI Timer.

11. List two distinct parts of any Hardware Platform Specification.

12. Which company developed AMBA and AXI?

13. List at least 3 functions of AXI Interconnect.

14. List at least 4 ports of an AXI-Stream Master (other than clk and reset), and divide them into inputs and outputs.

15. Name the system-on-chip bus standard recommended for use by opencores.org.

16. List at least 6 ports of an AXI-Full Slave (other than clk and reset), and divide them into inputs and outputs.

17. Explain the need for the volatile keyword in the following definition of Xil_In32():

```
u32 Xil_In32(u32 Addr)
{
    return *(volatile u32 *) Addr;
}
```

18. Which of the following operations (if any) can be omitted in case of the DMA-based communication between an ARM core and a hardware accelerator using ACP?

Write to Accelerator

- processor allocates buffer
- processor writes data into buffer
- processor flushes cache for buffer
- processor initiates DMA transfer

Read from Accelerator

- processor allocates buffer
- processor initiates DMA transfer
- processor waits for DMA to complete
- processor invalidates cache for buffer
- processor reads data from buffer

19. What operation starts a Simple DMA Transfer when using AXI DMA?
20. Explain the primary difference between Simple DMA transfer and Scatter-Gather DMA Transfer.
21. Which core can be used to simplify the development of an AXI-Full Master?
22. Explain the primary difference between DMA and Central DMA.

