ECE 699 Software/Hardware Codesign
Midterm Exam
Spring 2016

First Name: ……..
Last Name: ……..

Part 1: Concepts

1. List at least 3 advantages of implementing selected portions of a complex design in software.

2. What are the primary advantages of Zynq All Programmable SoC over a traditional FPGA, such as Virtex 7, with a soft microprocessor core, such as MicroBlaze?

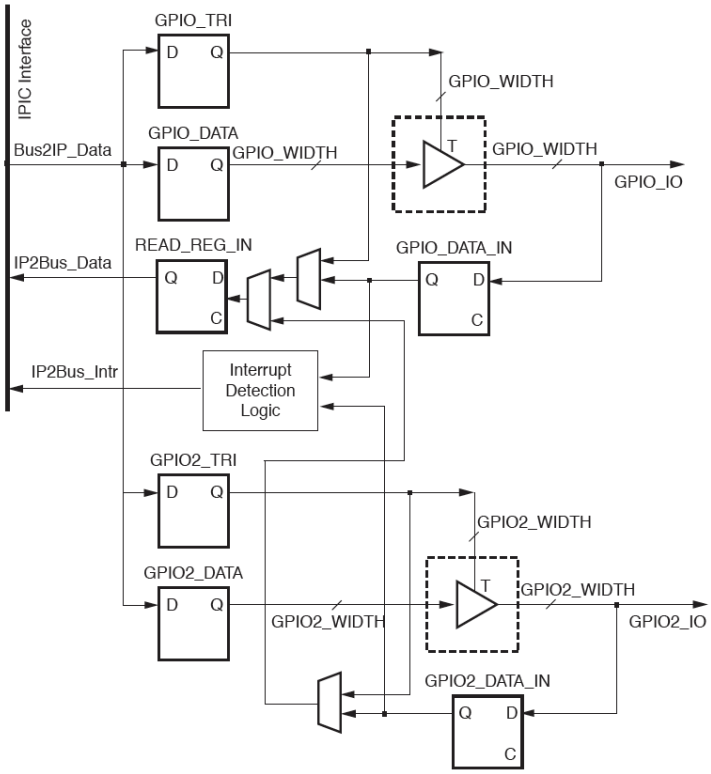
3. Explain the term differentiation, and describe how Zynq can be used to accomplish a high-level of differentiation.

4. List at least 4 major advantages of Vivado over ISE.

5. List 4 families of Xilinx devices supported by both Vivado and ISE.

6. How many different types of interrupts can be generated by the AXI GPIO core?

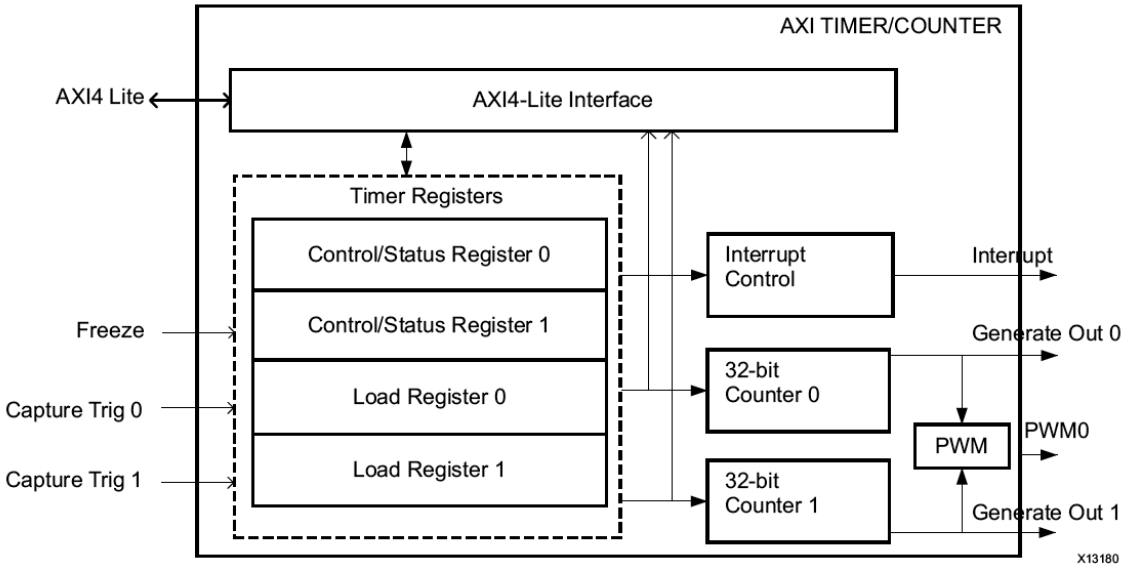
7. Explain the ways of minimizing the area of the GPIO core, shown conceptually in the diagram below.



8. Explain the role and functionality of GPIO_TRI registers, shown in the diagram above.

9. What are the primary limitations of the Accelerator Coherency Port (ACP) of Zynq, which go against the idea of full coherency.

10. Explain the operation of the PWM mode of the AXI Timer (shown in the diagram below).



11. Which mode of AXI Timer can be used to measure interval between two external events, such as two consecutive pushes of a button connected to the pins of PL?

12. Explain the difference between AXI Interconnect and AXI Interface.

13. Explain the primary differences between AXI Full and AXI Stream Interfaces.

14. Provide the names of at least two System-on-Chip Bus Standards competing with AMBA AXI4 standards.

15. Explain the need for the highlighted operations in case of the DMA-based communication between an ARM core and a hardware accelerator using GP Ports between PS and PL.

A. Write to Accelerator
processor allocates buffer
processor writes data into buffer
processor flushes cache for buffer
processor initiates DMA transfer

B. Read from Accelerator
processor allocates buffer
processor initiates DMA transfer
processor waits for DMA to complete
processor invalidates cache for buffer
processor reads data from buffer

16. Explain the meaning of each number in the following estimate of the maximum bandwidth supported by
    A. HP ports of Zynq:
    Maximum bandwidth = 4 * 64 bits * 150 MHz * 2 = 9.6 GByte/sec

    B. external DDR
    Maximum bandwidth = 1 * 32 bits * 2 * 533 MHz * 2 = 4.3 GByte/s

17. What operation starts a Scatter Gather DMA Transfer when using AXI DMA?

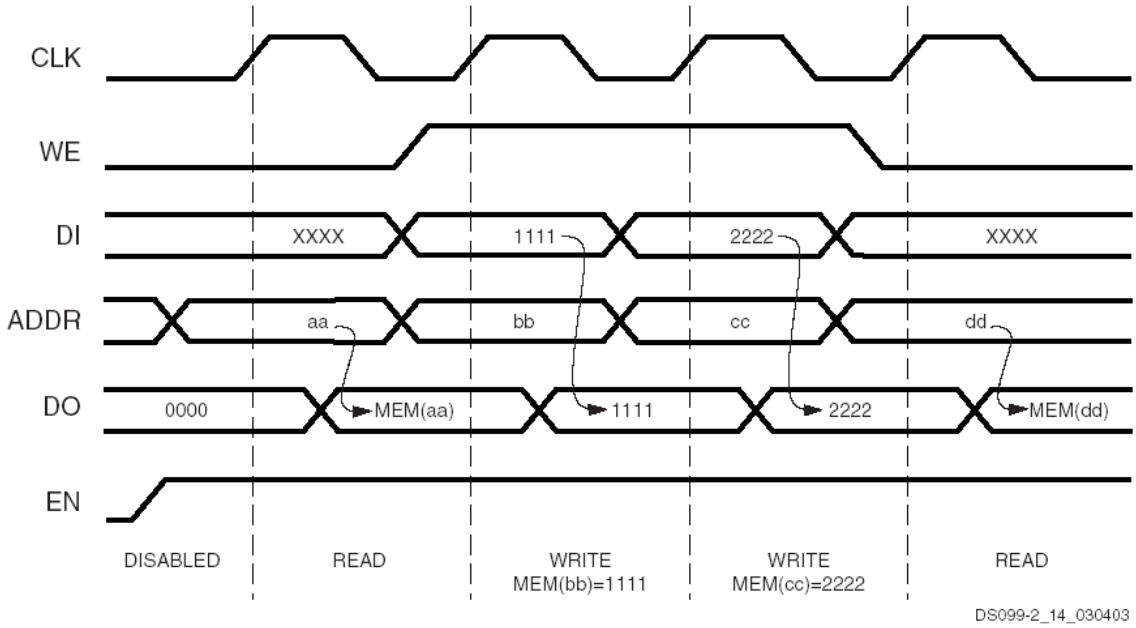
18. What is the primary advantage of using a Scatter-Gather DMA Transfer rather than a Simple DMA transfer.

19. Based on the table below calculate the latency in nanoseconds for communication between:

A. DMA and DDR, using HP interface
B. ARM and internal memory of AXI Slave located in PL, using GP interface

	L1 Cache	L2 Cache	DDR	OCM	IOP Slave	M_AXI_GP0
CPU Pipeline	1	25	67	20	122	86
Peripheral Master	–	–	136	106	–	126
S_AXI_ACP	27	32	89	27	124	–
S_AXI_HP0	–	–	76	46	–	–
S_AXI_GP0	–	–	118	88	144	–

20. Provide any missing fragments of the VHDL code describing Xilinx BRAM in the WRITE_FIRST mode, illustrated in the diagram below.




```
architecture behavioral of raminfr is
   type ram_type is array (0 to 2**r-1) of
                        std_logic_vector (w-1 downto 0);
   …… RAM : ram_type := (others => ……);

 begin
   process (clk)
   begin
     if (clk'event and clk = '1') then
       if (en = '1') then









       end if;
     end if;
   end process;



 end behavioral;
```

21. Explain the difference between Simple Dual Port RAM and True Dual Port RAM.

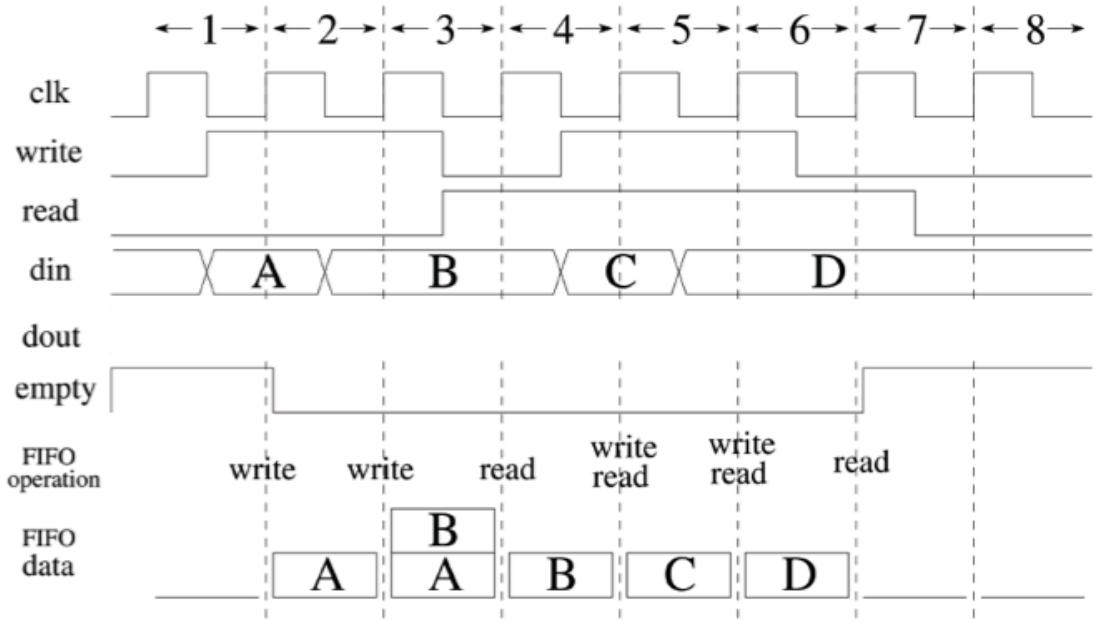
22. List at least 3 primary differences between distributed RAM and Block RAM in Zynq.

23. Determine the number of address bits, data bits, and parity bits in PORTA of a 36k BRAM configured as True Dual Port RAM, with 2048 memory locations.

24. Determine the number of MLUTs necessary to implement 128x8 Dual Port RAM.

25. Supplement the attached timing diagrams with the values of dout for

A. Standard FIFO



B. First-Word Fall-Through FIFO