Digital Optical Spectrum Analyzer  
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Abstract: An Optical Spectrum Analyzer (OSA) is an instrument for measuring the spectral characteristics of lasers. The most common examples are based on the Scanning Fabry-Pérot Interferometer (SFPI), which measures the intensity of an optical standing wave formed within a mirrored cavity. The analyzer’s control unit sweeps the resonant wavelength of this cavity at a fixed rate, and the intensity within the cavity is plotted against time to form a picture of the optical frequency spectrum. Commercial SFPI controllers widely used in physics research are analog systems and have many limitations. Team Spectrum has developed a low-cost stand-alone digital SFPI control system, compatible with existing SFPI hardware, offered as a drop-in replacement for analog controllers currently in use. This digital controller provides equivalent functionality at drastically reduced cost. This product is intuitive to operate, with a fully integrated user-friendly graphical interface, software that significantly simplifies measurement operation, and offers an automated setup process.

1. Introduction
The Scanning Fabry-Pérot Interferometer (SFPI) based Optical Spectrum Analyzer (OSA) is an instrument that displays the optical frequency spectrum of a laser. Widely used in experimental physics, the system consists of a SFPI cavity, a controller, and an oscilloscope (Figure 1). The SFPI cavity consists of two high-finesse confocal mirrors arranged to create an optically resonant cavity. One of the mirrors is attached to a piezoelectric motor, allowing a slight variation in mirror spacing to change the resonance frequency of the optical cavity. A photodiode detector, located behind the static mirror is positioned to measure transmitted intensity, which increases sharply as the cavity resonance frequency approaches the frequency of the incoming laser. In operation, the controller applies a ramping voltage to the piezoelectric motor, varying the resonant frequency of the cavity as a linear function of time. Peaks in field intensity within the cavity are transduced by the detector, amplified by the controller and displayed on an oscilloscope. OSA controllers are generally analog devices and limitations of their outdated designs are numerous, including system price (due to dedicated high-quality oscilloscope), complex controls, and manual operation. The goal of this project was to develop a digital version of an OSA characterized by automated continuous operations, low-cost, high accuracy for precise data acquisition, and an integrated display. Such a product would be useful in many areas of experimental physics, other sciences, as well as in industry.
2. Approach
To address these shortcomings, we have developed an innovative digital control system, compatible with existing SFPI hardware as a low cost drop-in replacement for the analog OSA currently in use. Our product, the Digital SFPI Controller, or DSC, offers numerous advantages ranging from utility and usability to enhanced accuracy and reduced maintenance, while costing much less than comparable products currently available on the market.

The DSC is a stand-alone OSA system with a dedicated Graphical User Interface (GUI) designed to display information relevant to the optical spectrum. The DSC is significantly easier to operate than existing controllers. Rather than varying several parameters of an analog ramp generator to select the visible portion of the spectrum, our digital system scans the entire range of the SFPI cavity at a constant rate. The user can then simply select the visible portions of the data set, using intuitive graphical controls. Algorithms within our product automatically adjust parameters, such as detector gain and offset voltage. The DSC can accommodate other SFPI cavities, however we constrained the design of the prototype to operation of the COHERENT cavity, set up with 1.5GHz FSR mirrors, as this model was readily available for testing.

3. System architecture
Figure 3 shows the system architecture of the DSC while Figure 4 shows the detailed design. The architecture enables the isolation of faults and allows for parallel development paths while still meeting all functional requirements. The system is comprised of five functional modules. The User Interface Module (UIM) is responsible for accepting control commands from a human operator, and managing the display and storage of collected data. This module consists of PC software, along with USB connectivity hardware shared with the Data Control Module (DCM). An embedded GUI utilizes the same USB-DCM interface as the PC, but includes a small HDMI LCD and tactile controls to allow the product to operate as a bench instrument. The DCM is responsible for accepting a control input and returning collected data to the UIM, providing an abstraction layer over the low-level high-speed interactions between output and input. The actual control over output and input, are time critical functions that must operate in exact synchronization at several hundred Megahertz. The Input Processing Module (IPM) is responsible for amplification of the detector in the SFPI cavity and A/D conversion. To meet the functional requirements, it includes a transimpedance instrumentation amplifier for photodiode input. The IPM also includes a low-pass filter and a high speed A/D converter. The SFPI Output Module (SOM) is responsible for digital-to-analog conversion, producing a high voltage (HV) analog output proportional to the magnitude of a binary input suitable for driving a piezoelectric motor. A low noise, high accuracy D/A converter, and HV (500V) supply and linear amplifier are also included in the SOM. The entire system is enclosed in a fabricated chassis with power supplies for various subsystems. This compact package is suitable for daily use in a lab environment.

4. User Interface Module (UIM)
The purpose of the UIM is to offer the Digital Optical Spectrum Analyzer (DOSA) operator intuitive and user-friendly control over all DOSA functionality, and present collected data in a simple and intuitive way. The UIM is a real-time embedded system responsible for: (i) configuring the DCM to collect data that the user has requested, (ii) retrieving collected data from the FPGA, and (iii) displaying and/or storing retrieved data. This process is repeated up to ten times per second. The main display uses the widely supported HDMI connector and has a standard resolution. The software has been tested on Arch and Debian Linux as well as Darwin (OS X), on both ARM and X86 architectures, providing cross platform versatility.
The real time graphing system was created by using software that utilizes GTK+ (gimp toolkit). The system also utilizes a GTK+ library called GTKDatabox, a library designed for real time graphs. The computer receives and interprets data through the libFPGAlink library from the analyzer’s central controller, the Data Control Module, or Atlys 6 FPGA. The computer is the heart of the User Interface Module (UIM). There are two USB systems connected to the computer. One of these connections is the FTDI USB bus which connects the user input hardware with the entire digital optical spectrum analyzer. The other interface is a USB cord connecting the computer to the Atlys 6 FPGA. This connection allows commands from the FPGA to reach the UIM. Finally, an HDMI cord allows the Lilliput 10” monitor to be available. This screen displays the user interface when the raspberry pi is the acting computer.

5. Data Control Module (DCM)
The Digilent Atlys demo board was selected for use in the DOSA prototype. The Atlys circuit board is a complete, ready-to-use digital circuit development platform based on a Xilinx Spartan 6 LX45 FPGA. The on-board collection of high-end peripherals, including Gigabit Ethernet, HDMI Video, 128Mbyte DDR2 memory array, audio and USB ports make the Atlys board an ideal host for complete digital systems. The User Interface Module (UIM) provides its user input signals to the DCM, and requires the DCM to provide data values and scan positions. The UIM uses the channel address to send scan values to registers in the FPGA. We utilized a USB connection from the UIM to
one of the two USB ports on the Atlys Development Board. The communication utilized the FX2 chip to program the FPGA, the communication code being provided by FPGA link with some slight modifications. In order to use the chip, however, the FX2 required generating a bitstream file, then a boundary scan file or XSVF file, generated by Xilinx Impact. Once the XSVF file was generated, the FPGA was programmed and controlled from the UIM. When all of the appropriate files were in place, we were able to use the FX2 to program the FPGA from the User Interface while being controlled by a laptop and a command line. A high performance FPGA (Xilinx Spartan 6) was used as the core of the DCM.

The DCM logic as implemented as a finite state machine (FSM) in order to properly send correct scan values to the SFPI Output Module. The FSM sits in an idle (wait) state until the UIM sets the DCM command register to “START SCAN” via USB. At this point, the FSM latches the configuration settings into internal registers for the duration of the scanning process. A number of validation checks are performed on this data, and the FSM has three error states assigned to (1) oversampling that exceeds allocated memory (2) errors that result in too large of a step size and (3) a stop value higher than the start value. For example, if the minimum scan position was greater than the maximum scan position, the FSM would fault to an error state and return to the user input wait state. Another data flow program separate from the FSM was the DDR2 memory controller. This controller utilized a small FSM to determine timing characteristics, determining when values should be written to and read from memory. The memory controller, provided by Xilinx Coregen had a data path, control and read and write FIFOs that would hold data until a read or write command was given. Finally, all of the components were tied together in a top level VHDL file.

Each VHDL file that comprised the DCM was test benched individually before integration into the top-level design. In addition, the DCM as a whole was tested. The first test was completed when we established communication between the Data Control Module (DCM) and the User Interface Module (UIM). A second test was an extension of the first pertaining to communication. After the finite state machine (FSM) was completed, a block RAM was created to replicate data arriving from the Input Processing Module (IPM) FIFO. This allowed us to internally send data we could control to the module which in turn allowed us to predict the expected behavior of the FSM. To initialize the test, a read command was sent with proper scanning parameters from the User Interface Module (UIM) to the Data Control Module. This test was taken a step further, where the data was read back into the UIM from the DCM, successfully producing a graph on the interface monitor as depicted below.

![Figure 5: One of the 19 test benches that were developed to verify the DCM functionality](image)

**6. Input Processing Module (IPM)**

The Input Processing Module is responsible for amplifying the photocurrent produced in the SFPI photodiode and converting it into a digital form. No commercial products meeting the required specifications for the amplifier could be located, so an original design was created and implemented.

The photodiode in the SFPI produces a very small signal, in the µA to mA range, and transports it over a coaxial (unbalanced) cable. This constraint presented a number of issues that are addressed by our design. The amplifier is a novel design featuring an isolated floating instrumentation input, differential output, and 16 digital gain steps ranging linearly from 5kΩ to 900kΩ programmed over a protected four-wire LVTTL-compliant serial interface. It
requires only ±5V supplies at less than 20mA per rail. The basic amplifier design utilizes a resistive T-Feedback
architecture to reduce DC offset error. This design also allows the use of much smaller resistances, reducing
voltage noise. We chose the Linear Technology LT1886 dual-SOIC op amp based on a 700MHz GBP, low output
resistance, and outstanding noise performance. For the variable gain design, we developed a binary-weighted
shunt using the ADG714 analog switch and four resistances per channel.

Converting this into a digital signal and sending this signal to the Data Control Module (DCM), we broke the
module into a two-part design. The first part is the transimpedance gain amplifier and the second part is the
analog to digital convertor with a resolution of 16 bits. The transimpedance gain amplifier takes in an analog
current signal from the SFPI cavity and converts it to a voltage that can be used by the analog to digital convertor.
The transimpedance gain amplifier portion proved to be the most difficult to design.

The last half of the Input Processing Module (IPM) consisted of the ADC and was fairly straightforward in
comparison to the VGA half of the module. The ADC we chose was the Linear Technology LT2203. This component
was a 16 bit high-speed converter, capable of accepting a large number of samples, and of handling high numbers
for each sample. With this last half, we were able to complete the overall circuit design by adding power
regulation, a way to communicate with the switch, connections to the analog to digital convertor, and a
connection from the SFPI cavity.

Figure 6: Input Processing Module; schematics, a PC board design, and final module
IPM testing consisted of SPICE simulations and physical testing. Spice simulations were extremely useful, and were used to calculate frequency response, DC characteristics, and to characterize the performance of various Op Amps. We used LTSpice software, provided by Linear Technology due to the vast built-in library of high-performance Op Amps.

![Graph](image)

**Figure 7**: Input Processing Module (IPM) Graph, gain of the input versus the gain of the output. Note that for a certain range of inputs the gain produced at the output on the x axis is a single value, a step.

Once the simulations were complete, we built and tested the physical module. Our first test was to see if data was being transmitted on the output of the transimpedance gain amplifier. To test this, we used a laser diode as the input in place of the SFPI cavity, the laser being easier to control and gain access to. An Arduino Board was connected and coded to provide the gain step signals. The output of the circuit was monitored with an oscilloscope. Once we confirmed that the received signals were showing the appropriate behavior, we moved on to testing the circuit with the real SFPI cavity, were the test with the cavity also turned out to be successful.

**7. SFPI Output Module (SOM)**

The SFPI Output Module is responsible for producing high voltage. This high voltage is necessary to drive the piezoelectric motors in the SFPI cavity. To make this output meaningful, it needed at least a command as an input to instruct when to provide a ramp function from 0 to 500V as an output, and when to stop producing this ramp. Also, due to its high voltage nature, this module was responsible for monitoring the output internally. For safety reasons it must be able to monitor the output and shut it off or short it to ground as quickly as possible to prevent any potential hazards. Also, for ease of testing and safety, this module was further broken down into two halves which included a high voltage section and a low voltage circuit.

The majority of the high voltage section is handled by the PiezoMaster, taking care of amplification, monitoring, noise reduction, and some safety. We decided that a little redundancy in the safety features would be desirable. Aside from the PiezoMaster’s internal safety features, an extra disconnect and crowbar were added to the amplifier’s output. The disconnect is handled by a relay that physically cuts off the high voltage from reaching the output port. This relay, though relatively fast, would still leave the output high for a few milliseconds. To cut down this time, a crowbar was added with a design to react much faster.

The schematic for the low voltage circuit is shown in Figure 8. The low voltage circuit design is responsible primarily for converting the input of the Digital Control Module into analog signals that are sent to the amplifier. Its secondary job, however, is to serve as a pre-high voltage monitoring system. To accomplish both of these tasks, the circuit relies on two major components: a digital to analog converter (DAC), and a microcontroller. We decided on a DSP1791 for the DAC due to its low noise and muting ability. The muting feature would serve as a way for us to block the digital signal from being converted and output inside the DAC itself. The microcontroller is in charge of monitoring the output signal for problems, and initializing and controlling the DAC. The ATTiny 261 was selected...
because it was a fairly simple microcontroller with enough I/O Ports to complete the task.

The last major section of the low voltage circuit is a voltage shift circuit at the DAC's output. This circuit designed from operational amplifiers was in charge of changing the voltage range of the DAC from -1.7V to 1.7V into the range 0 to 3.2V. This 0 to 3.2V is the input range that the amplifier component, the PiezoMaster, was expecting to see. The remainder of the circuit was designed to allow programming of the microcontroller, FPGA access for inputting clocks, data, and space for flags to be sent by the low voltage circuit, voltage sources, and allow for easy testing and error detection. This circuit was tested in a DC Sweep, an AC Sweep, and for noise. The results produced the three graphs shown in Figure 9. The gain and phase demonstrated a stable system, where the voltage range was corrected to 0 to 3.2V as required for the output of the low voltage circuit, and the noise at output even with high input noise was negligible.

Figure 8: SFPI Output Module Low Voltage Circuit Schematic and PC board

Figure 9: Test results for voltage shift circuit: output voltage graph, gain graph, and noise graph
Further tests on the low voltage circuit occurred once the board and components were assembled. The voltage supplies on board were tested and found operational. The output of the DAC was tested while idle to determine the voltage offset and current draw. The offset was found to be about 20mV, with the idle current being approximately 10mA on the negative rail and 80mA on the positive rail. A few more power and ground tests were completed and the circuit deemed fit for testing the converter with signals. Code was written for the microcontroller to test its operation before using it to program the digital to analog converter (DAC), using four on-board LEDs that were designed onto the PCB. Once this test code was working, code for the DAC control was generated.

When testing the High Voltage half of the module, we first grounded the circuit’s output and applied only control signals to the SCR and Relay to monitor the disconnect and crowbar reactions. Once these safety features were tested, we moved on to test the PiezoMaster itself to see if dummy input values in the 0 to 3.2V range placed directly into the amplifier would produce the desired high voltage output.

8. System Testing
After all module tests were complete, we tested the entire system. This testing was conducted in a Physics lab at GMU. First, the external analog OSA (the equipment we hope to replace with the DOSA) was used to verify that the laser was operating in single mode. Then, the photodiode output from the SFPI was disconnected from the analog OSA and connected to the IPM VGA. In this configuration, there was no synchronization between the output ramp and the screen, so the image was not very steady. However, this was to be expected. This configuration demonstrated that all of the input subsystems worked correctly despite the unsteady image, which would be addressed when the system was put to its final test. The second system test was to connect the PD output back to the analog OSA, disconnecting the inputs. Then the ramp output from the SOM-HV was connected to the SFPI, allowing the DOSA to ramp the cavity and see if the outputs were behaving as expected. This test passed as well, with the external analog OSA showing the same peaks as it did before. During the third system test (the overall test) the analog OSA was disconnected all together, and the DOSA was connected to both the SFPI output and photodiode input. In this test, the DOSA was responsible for all elements of the design requirements. The DOSA display matched that of the Analog OSA used before, thus demonstrating that the system developed by the team worked as specified.