Notice and Invitation

Oral Defense of Master's Thesis

The Volgenau School of Engineering, George Mason University

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Spatial and Temporal Scheduling of Clock Arrival Times for IR Hot-Spot Mitigation, Reformulation of Peak Current Reduction

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Physical Design Automation Tool

Monday, July 17th, 2017, 2:30pm

Room 3202 Engineering Building

All are invited to attend.

Committee

Dr. Avesta Sasan, Thesis Director

Dr. Jens-Peter Kaps

Dr. Xiang Chen

Abstract

One of the major reason for chip failures is on chip variability. In order to prevent failures due to on chip variability, the variability need to be margined in physical design by providing voltage guard band. One of the major reasons of variability is dynamic IR drop. To prevent the timing failures due to large IR drop, big margin is provided as voltage gaur band. So by reducing IR drop the timing failures can be avoided and this gives option for reducing the voltage gaur band margin. In this thesis we propose a technique to reduce the IR drop by temporal scheduling of clock arrival times for IR Hot-Spot mitigation. In this technique we utilize the available slack and scheduling useful skew we distribute the switching of cells within the timing window. Previous work done for reducing the IR-drop was focused on reducing the overall peak current but we breakdown the problem into many smaller problems of local IR-hotspots. And based on location of the cells we group them based on minimum resistive region and change the clock arrival time of the flip flops for reducing the intensity of individual hot spots. Application of the proposed solution to a selected number of IWLS benchmarks reduces the peak IR-drop by ~35%, and peak current by ~37%

Complete Physical design process involves various tools like Design compiler, Primetime, ICC and needs many scripts to be implemented and executed. And complete Physical design process is time consuming and based on the size of the design. To automate the physical design process across all tools used a tool was implemented based using GNU make. Using this Physical design automation tool all the physical design steps like Synthesis, Floor-planning, Placement, Clock Tree Synthesis, Routing and STA analysis was automated.