Implementation of Log-Domain FFT Based LDPC Decoder on a GPU

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Forward error correction enables reliable one-way communication over noisy channels by transmitting redundant data along with the message in order to detect and resolve errors at the receiver. Low-density parity-check (LDPC) codes achieve superior error-correction performance using belief propagation (BP) decoding. However, the computational complexity of a BP decoder is $O(q^2)$ operations for each checksum calculation, where q represents number of symbols in the underlying Galois field. The complexity is reduced by transforming the operations into the log and frequency domains. This thesis explores how a GPU implementation of a Log-domain FFT based LDPC decoder performs in comparison to a CPU implementation for regular MacKay construction. Numerical results show that the GPU implementation is about twice as fast as the CPU implementation. The thesis also studies the performance of GPU implementations of a Quasi-cyclic LDPC decoder for WIFI (IEEE 802.11n) and WIMAX (IEEE 802.16e) LDPC codes.