In high performance computing, an important element of the overall system performance is the network interconnects that connect multiple computing nodes. PCI Express (PCIe) has been widely adopted as a high throughput bus to meet the bandwidth demands of modern computing devices. An important application in the field of cryptography is adoption of the PCIe bus to connect custom cryptographic accelerators in FPGAs to user space applications. In particular, the HardwaRe Module Evaluation System (HeRMES) is being developed by the GMU CERG group as a platform for evaluation of several cryptographic FPGA implementations. At a high level, this process includes attaching the cryptographic module to the DMA controller and the PCIe interface IP on the FPGA. In addition, appropriate kernel driver and user space library is required. This paper presents an overview of the PCI Express architecture and topology, along with its key features and advantages. It then describes the hard IP cores available on three modern FPGAs from Xilinx and Altera that implement multiple layers of a PCI Express bus. Finally, the paper presents adoption of EZDMA2 and QuickPCIe custom IP cores provided by PLDA. These IP cores will be utilized on three FPGA prototype boards for the HeRMES project.