GEORGE MASON UNIVERSITY
ELECTRICAL AND COMPUTER ENGINEERING
LABORATORY RULES

1. There will be **NO FOOD OR DRINKS** in the laboratory at any time. Students will be held liable for any damage to equipment resulting from abuse of this rule.

2. Students are not allowed in the laboratories without a Lab Instructor or Lab Monitor present, unless signed in with the Lab Manager. Open lab times for make-up or project work will be posted. When a Teaching Assistant is holding office hours, he/she is also monitoring an open lab which any student may use. ECE/CpE students have priority in the Computation and Test Lab, Room 265, ST II.

3. If you suspect a problem with the equipment, notify the TA or Room Monitor. Then, either leave a note on it with a brief description of the problem/symptoms, or bring the equipment to the Lab Manager, Room 120D, ST I.


5. **YOU are responsible for leaving your workstation clean and in good condition when you leave.** Failure to do this will negatively impact your final lab grade.

Before leaving:

   a. Hang up all test leads neatly under appropriate connector combination.

   b. Tidy workstation.

   c. Throw away all trash.

   d. TURN OFF equipment and lab table SWITCHES.

This is a non-smoking university. This building has **NO** designated smoking areas so you must go outdoors if you choose to smoke.
ELECTRONICS SAFETY

Exercise of good judgement and knowledge will ensure you a safe laboratory experience.

Do not defeat any safety device such as a fuse or circuit breaker, by shorting across it or by using a higher amperage fuse than that specified by the manufacturer.

Avoid direct contact with any voltage source. Do not wear rings, watches, bracelets, or dangling necklaces while working on equipment. Do not grasp any exposed metal in your circuit when the power is on.

Keep hands dry. Water and perspiration increase conductivity.

Wear shoes with insulating soles.

Measure voltages with one hand held behind you or in your pocket.

Avoid eye injury when cutting off excessive wire lengths. Point the wires downward toward your table top so the cut pieces cannot fly toward your eyes or another person’s.

Shut off the power when connecting components or test equipment to a circuit. Double check your wiring before you apply power.

Make sure your circuit is properly grounded. Beware of a possible floating ground. It is a good idea to connect all grounds together before applying power.

To prevent power terminals from shorting, keep the leads coming from those terminals apart.

Your exercise of common sense, safety precautions and knowledge will help you avoid the dangers of electricity. The amount of current required to become lethal depends upon:

1. the person involved and state of health,
2. area of the body involved,
3. length of time the shock is received, and,
4. type of electrical current.

Severe electrical shock will cause burns and/or paralysis. A small current passing through the chest can kill. With even minor electrical shock, some people react by going into traumatic shock.

In case of accident, turn off power immediately and call 911. If you suspect someone is touching a “live” wire, do not touch them. Use something non-conductive to push, rather than pull, them away from the wire. An injured person should be kept lying down until medical personnel arrive, and should be kept warm to help prevent traumatic shock. Be sure nothing is done to cause further injury.
1. Instruction manuals for the laboratory equipment may be checked out in room 120D, S&T I. It is essential that you become familiar with the correct way to use the basic equipment in your first lab course. Wire cutters/strippers are available for sale or you will need to bring your own.

2. Twenty-two gauge wire (22AWG) is the best size to use with the trainers and solderless breadboards. Solid wire only, never stranded, is used for the trainers. There are spools of wire cabled to the back shelf. You will need to cut some and strip the insulation at both ends.

   Keep jumper wires short. Strive for a neat and logical layout. This will make troubleshooting easier and successful circuits more likely. (See ex. posted in lab.)

   Strip no more than approximately 3/8 inch of insulation from your jumper wires. Exposed wire increases the risk of short circuits.

3. Using more than one color of wire will help you debug your circuits. Normally RED and BLACK are reserved for power and ground.

4. Probe tips should not be inserted into the solderless breadboard. Wrap a wire around your probe hook tip twice for stability and insert the other end into the connector block. Alligator clips on the equipment leads also need a wrapped wire for connection to the trainers and breadboards.

5. Always ground your probe, but keep the ground wire short. Use the method of wire wrapping described in the previous tip to attach to the alligator clip of the probe ground wire.

6. For any potentiometers (such as most multiturn) which require adjusting, a trimpot tool is available for purchase from room 120D, S & T 1. It is included in appropriate kits.

7. Most of the chips used in your lab are not overly static sensitive. However, you should observe some precautions when handling them. If you were issued a tube, it protects the chips from static charges, and is sturdy enough to provide protection to the delicate, metal pin legs.

8. Keep your chips away from magnets, motors and high temperatures. Don’t leave them in your car in the sun or extreme cold. They do best in the moderate temperatures most humans prefer.

9. Bent pins may be gently straightened with fingernails or a needlenose pliers. If the pins break, you will need to purchase a new IC.

10. A small, narrow-blade, flathead screwdriver is useful in removing chips from breadboards. Using a side-to-side rocking motion as you insert the blade under the chip, keep a finger lightly on top of the chip to prevent it suddenly popping up on one end, bending the pins.
11. To locate pin 1 on an integrated circuit (IC, chip), look for one of the following:

- A semicircle at one end, often cut into the end of the chip - With this at the top, pin 1 is at the left of the half circle. Sometimes, there is one whole circle.

- A tiny spot in the corner of the chip beside pin 1 - There may or may not be other marks on the chip.

Always count pins from pin 1 around the chip so that the last pin is straight across from pin 1. Common chip sizes are 8 pin, 14, 16, 18, 20, 24, 28, and 40 pin. Your TTL ICs (Transistor-Transistor Logic Integrated Circuits) will be in dual inline packages (DIP).

12. Chip leads are slightly flared to help hold them in printed circuit boards while being soldered. You will need to reduce the flare to allow them to be inserted into the breadboard. Use a pair of needle nose pliers or press the leads against a table top while rotating the body of the chip towards the lead points to reduce the lead angle of all evenly. Don't bend too far; there is no easy correction.
Laboratory Report Format

1. Cover Page
   a. Course Number
   b. Experiment Number and Title / Name of Experiment
   c. Your Full Name
   d. Date of Submission

2. Objective of your Experiment
   State the objective and what you are trying to prove. This should be general and is intended for a reader with moderate background knowledge.

3. Theoretical Background
   Describe in brief conceptual and theoretical background of the circuit(s) of the experiment.

4. Circuit Diagrams
   Draw clearly with proper label all the circuits you built in the experiments.

5. Materials and Equipment
   List all the components and Equipments you use for the experiments.

6. Laboratory data
   This Section is for your collected data, along with plots, tables and illustrations.

7. Theoretical Data
   Include any data that you can predict, corresponding to your collected laboratory data, using mathematical models, equations and laws.

8. PSPICE Simulation Results
   Place all PSPICE simulation results, including PSPICE Circuit, simulation profile.

9. Comments and Conclusion
   Discuss what went as expected and what did not. Compare your theoretical, laboratory and PSPICE result. Discuss how closely they are same and why there is any variation, if any.

Make sure that all of the questions in the lab manual are answered completely. Be creative. Try to explain as much as possible, yet be concise.
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LAB 1
RC PASSIVE FILTER

The purpose of this lab is to understand different types of passive filters and to learn their working, characteristics and frequency response.

Concept

The RC passive filter is one of the basic building blocks of both signal processing and communication circuits. Its main purpose is to allow certain frequencies to pass, while it blocks other frequencies. These types of filters allow us to extract the information that we desire from an incoming signal comprised of many different frequencies. Two basic types of filters are Low Pass Filter (LPF) and High Pass Filter (HPF).

An ideal LPF allows signal up to a certain frequency, called cut-off frequency, $f_c$, to pass through the circuit and block any frequency above $f_c$. In the passive LPF shown in Fig. 1.1(a) the capacitor reactance ($X_c = \frac{1}{2\pi f_c}$) is high at low frequencies resulting in a high output voltage. As the frequency increases the $X_c$ decreases and consequently the output voltage also decreases. Figure 1.1b shows frequency response plot of a LPF.

Similarly an ideal HPF (Figure 1.2a) allows frequency above $f_c$ to pass through the circuit and blocks any frequency below $f_c$. At high frequencies the reactance of the capacitor drops and hence allows high frequencies to pass through it to the load (R). Figure 1.2b shows frequency response plot of a HPF.

The cut-off frequency depends on the values of the resistor, R and capacitor, C and is determined by the formula, $f_c = \frac{1}{2\pi RC}$

The impedance, $Z_c$ of the capacitor is given by $Z_c = \frac{1}{\omega C}$ where $\omega = 2\pi f$ is called angular frequency. The voltage $V_o$ in a LPF can be expressed as $\frac{V_o}{V_i} = j\frac{Z_c}{R+jZ_c}$. The magnitude of the transfer function (gain) of the LPF can be expressed as given below.

$$|\frac{V_o}{V_i}| = \left|\frac{\frac{1}{\omega C}}{R + \frac{1}{j\omega C}}\right| = \left|\frac{1}{1+j\omega RC}\right| = \frac{1}{\sqrt{1 + (\omega RC)^2}}$$

The magnitude of the transfer function (gain) of the HPF can be expressed as given below.

$$|\frac{V_o}{V_i}| = \left|\frac{j\omega RC}{1+j\omega RC}\right| = \frac{\omega RC}{\sqrt{1 + (\omega RC)^2}}$$

The phase difference of $V_o$ and $V_i$ of a LPF is given by $\phi = -\tan^{-1}(\omega RC)$. The phase difference of $V_o$ and $V_i$ of a HPF is given by $\phi = \frac{\pi}{2} - \tan^{-1}(\omega RC)$. If we plot the gain in decibels, we can define the 3 dB cutoff frequency as the point where the gain (dB), $20\log_{10}\left|\frac{V_o}{V_i}\right|$, falls by 3dB from its maximum value. In other words it is the frequency where the gain reduces to 0.707 times the maximum value.
Experiment

1.1a RC Low Pass Filter

1.1b Frequency Response of Low Pass Filter

NOTE: The dotted line represents the ideal filter response. The solid line is the response of an RC filter. The steeper the slope of the practical filter, the closer it becomes to being ideal and the better it is.

PART A- RC Low Pass Passive Filter

1. Build the RC low pass filter circuit as shown in Figure 1.1a. Set R at 10 KΩ and C at 0.01 µF.
2. Apply $V_{in} = 1V_{pp}$ and measure frequency response of the amplitude of the output signal from 1 KHz to 1 MHz. At each frequency also measure phase of the output signal with respect to the input signal.
3. Plot amplitude of Gain (dB) vs frequency and Phase vs frequency graphs on a semilog graph paper. Logarithmic axis should be the frequency and linear axis should be either the amplitude of gain (dB) or the phase.
4. Calculate $\frac{V_o}{V_i}$ and phase from the formulae given before and plot the calculated gain (dB) v frequency and the calculated phase v frequency on the same semilog graph paper.
5. Extract 3dB cut-off frequency for both measured and calculated plots.
6. Verify result using PSPICE. Attach the printout of your PSPICE work.
7. Compare and show your results in a tabular form (include the measured results, the calculated results and the PSPICE results).
PART B

1. Repeat PART A with a new value of R provided by the TA.

PART C - RC High Pass Passive Filter

1. Build the RC high pass filter circuit as shown in Figure 1.3. Set R at 10 KΩ and C at 0.01 µF.
2. Apply $V_{in} = 1V_{pp}$ and measure frequency response of the amplitude of the output signal from 1 KHz to 1 MHz. At each frequency also measure phase of the output with respect to the input signal.
3. Plot amplitude of Gain (dB) vs frequency and Phase vs frequency graphs on a semilog graph paper. Logarithmic axis should be the frequency and the linear axis should be either the amplitude of gain (dB) or the phase.
4. Calculate $\left| \frac{V_o}{V_i} \right|$ and phase from the formulae given before and plot calculated gain (dB) v frequency and calculated phase v frequency on the same semilog graph paper.
5. Extract the 3dB cut-off frequency for both measured and calculated plots.
6. Verify the result using PSPICE. Attach the printout of your PSPICE work.
7. Compare and show your results in a tabular form (include the measured results, the calculated results and the PSPICE results).

PART D

1. Repeat PART C with a new value of R provided by the TA.

Question

1. Design a band pass filter using one low pass and one high pass filter with cut-off frequencies at 3 KHz and 7 KHz. Verify your design with PSPICE. Show all work and attach printout of the PSPICE.
2. For each filter discuss how the response change when the values of R and C are changed (both increased and decreased).
LAB 2
DIDOE CHARACTERISTICS

The purpose of this lab is to study the current – voltage (−V) characteristics of silicon p-n diode, germanium p-n diode, Schottky (metal-semiconductor) diode and Zener diode.

Concept

A diode is a two-terminal device formed by bringing n-type and p-type materials (or a metal and a semiconductor in case of a Schottky diode) together, which allows flow of current in one direction and blocks the flow in opposite direction. It comprises of a anode terminal and a cathode terminal, as shown in Figure 2.1

![Diode and its symbol](image)

When a positive voltage is applied to the anode (with respect to the cathode), the diode is said to be forward biased. When a negative voltage is connected to the anode (again, with respect to the cathode), the diode is said to be reversed biased.

Practically, in forward bias, when the applied voltage is less than the cut-in voltage (Vᵣ), there is only a small current flow through the diode. When applied voltage is higher than the cut-in voltage then there is a rapid increase in the amount of current flow through the diode. In reverse bias, there is a very small current called reverse saturation current, Iₛ, that conducts through the diode. This current is mainly due to the flow of minority carriers and it is called the leakage current. As we increase the reverse biased voltage, junction breakdown occurs at a voltage known as the breakdown voltage, Vᵦ. At this point current will increase sharply and diode is deemed to be in breakdown region (see Figure 2.2).

Current flowing through a diode, Iₔ, is given by

\[ I_ ISIL = I_s \left( e^{\frac{V_ ISIL}{nV_t}} - 1 \right) \]

where
- Iₛ is saturation current
- Vₛ is voltage across diode
- Vₜ is thermal voltage
- n is an ideality factor between 1 and 2, depending on fabrication process and semiconductor material. In most cases it is assumed to be equal to 1 and hence n is not mentioned.

Manufacturing techniques, fabrication processes and material properties determine the characteristics of diodes. In this lab we will study how diodes of different material behave differently.

Zener diode is a special type of diode which works very similar to the conventional diode but it exhibits controlled breakdown characteristic. In a zener, in the breakdown region, the current changes abruptly while the voltage remains close to the rated breakdown voltage.
Experiment

PART A – Silicon pn Junction Diode

1. Using an Ohmmeter identify the anode and cathode terminals of the Silicon diode (IN4002). Which electrode does the band refer to?
2. Build the circuit as shown in Figure 2.3 and connect the multimeters appropriately to measure $V_d$ and $I_d$.
3. Measure the $I - V$ characteristics ($I_d$ vs $V_d$) of the diode.
   a. To measure the reverse bias characteristics, vary $V_{in}$ such that $V_d$ changes from 0 V to about -15 V in steps of 1 V. Measure $I_d$ at each reverse bias voltage value.
   b. For measuring forward bias characteristics, vary $V_{in}$ such that $V_d$ varies from 0 V to a MAX VALUE corresponding to an $I_d$ value of 10 mA. Choose voltage $V_d$ steps of 0.1 V until you reach the cut-in voltage (~0.6 V) and then increase $V_d$ value in smaller steps to record all features of the diode $I - V$ characteristics.

NOTE: MAX Voltage for $V_d$ will be between 0.7 V and 0.9 V depending on the series resistance of the diode.
4. Calculate the theoretical current values for each $V_d$ using diode current equation. Use the value of $I_s$ as given in datasheet. Check if the data sheet $I_s$ value agrees with $I_s$ value you calculate from the experimental data.
5. Plot the measured and the theoretical $I - V$ characteristics on the same axes.
6. Verify and compare your results with PSPICE. Show your results in a tabular form and discuss if there are any differences among the three results (experimental, theoretical and PSPICE).

PART B – Germanium pn Junction Diode

1. Repeat PART A for the Germanium diode (IN270). Remember the cut-in voltage of the germanium diode is smaller than that of the silicon diode. Hence, go with smaller forward bias voltage steps for the germanium diode.
PART C – Schottky Diode

1. Repeat PART A for the Schottky Diode (IN5817). Note that the cut-in voltage is smaller for the Schottky diode as well compared to the silicon pn junction diode. Hence, go with smaller forward bias voltage steps for this diode.

PART D – Zener Diode

1. Using an Ohmmeter identify the anode and cathode terminals of the zener diode (1N751A). Which electrode does the band refer to?
2. Build the circuit as shown in Figure 2.4 with multimeters connected appropriately.
3. Measure $I - V$ characteristics ($I_z$ vs $V_z$) of the diode.
   a. For reverse biased characteristic vary $V_{in}$ such that $V_d$ varies from 0 V towards negative voltage in steps of 0.5 V until you reach breakdown and in smaller steps within the breakdown region. Measure the diode current at each step. The voltage across the diode and the current flowing through the diode in the breakdown region are designated by the symbol $V_z$ and $I_z$, respectively.
   b. For forward biased characteristics vary $V_{in}$ such that $V$ varies from 0 V in appropriate steps. Measure the current at each step.
4. Plot the measured $I - V$ characteristics on the graph. Determine the $V_{zo}$ by extrapolating the $I - V$ characteristics in the breakdown region on to the voltage axis. Find the $r_z$ value from the slope of the $I_z - V_z$ characteristic in the breakdown region and also by substituting $V_{zo}$ value and a $(V_z, I_z)$ datapoint into the equation $V_z = V_{zo} + r_z I_z$.
5. Generate a theoretical plot of $I_z - V_z$ using the equation $V_z = V_{zo} + r_z I_z$.
6. Compare the theoretical plot with the experimental plot. Do you see any deviation between the plots? If so why?
7. Verify and compare your results with PSPICE. Show your results in a tabular form and discuss if there are any differences among the three results (experimental, theoretical and PSPICE).

![Figure 2.4 Zener Diode Characteristics](image)

Question

2. What is the Max diode Voltage ($V_d$) you reached in step 3b of PART A, PART B and PART C? Explain why you could not go beyond this Max Voltage.
3. Design a shunt regulator using a zener diode for the following specifications: $V_z = 6.8$ V, $r_z = 5 \, \Omega$ at $I_z = 20$ mA. Supply voltage is 9 V. Verify your design using PSPICE.
LAB 3
RECTIFIER CIRCUITS

The objective of this lab is to understand the characteristics and the working of half-wave, center-tapped and bridge rectifier circuits.

Concept

One of the most important applications of diodes is in the designing of rectifier circuits. As you have already learned in Lab 2, diode allows current only when it is in forward biased mode. Thus, when an ac voltage is applied to a diode, the diode is forward-biased for one half of the cycle, letting the signal to go through it; and reverse biased for the other half of the cycle, blocking the signal. Hence, the output waveform will be a pulsating unidirectional waveform as shown in figure 3.1.

![Figure 3.1 Rectifier Input-Output Waveforms](image)

Using this property of the diode, first stage of the rectifier circuit is designed to convert an ac signal into a pulsating unidirectional signal. Three basic rectifier circuits are the half-wave, the center-tapped transformer full-wave and the full-wave bridge rectifier circuits. Half-wave rectifier allows only the positive cycle of the input ac signal to pass through and the negative input ac signal is blocked. A full-wave rectifier allows both the positive and the negative input ac signal to pass through. Negative half cycle is inverted at the output. Thus, we get a continuous pulsating unidirectional signal.

You will use a step-down transformer in this experiment. The transformer consists of two separate coils wound around an iron core that magnetically couples the two windings. The primary winding, having \( N_1 \) turns, is connected to an ac supply, \( V_p \). The secondary winding, having \( N_2 \) turns, will develop voltage \( V_s = V_p \left( \frac{N_2}{N_1} \right) \) between the two terminals of the secondary winding. See Figure 3.2.

![Figure 3.2 Transformer symbol](image)
Experiment

Use Silicon Diode IN4001 for this lab.

Part A – Half-wave rectifier

1. Build the circuit as shown in figure 3.3. Do not connect the transformer (F192X) to the circuit at this time.
2. Now connect the transformer to a function generator. Keep the function generator amplitude at its maximum at 1 KHz and measure the voltage, \(v_s\), between the secondary winding.
3. Connect the transformer to the rectifier circuit built in step 1.
4. Observe the secondary winding waveform and the rectified output waveform together on an oscilloscope.
5. Measure and record your observations.
6. Verify your results using PSPICE.

Part B – Center-tapped transformer full-wave rectifier

1. Build the circuit as shown in figure 3.4. Again do not connect the transformer to the circuit at this time.
2. Repeat step 2 to step 6 of PART A

Part C – Full-wave bridge rectifier

1. Build the circuit as shown in figure 3.5. Again do not connect the transformer to the circuit at this time.
2. Repeat step 2 to step 6 of PART A
Part D – Voltage Doubler

1. Build the circuit as shown in figure 3.6
2. Provide $V_{in} = 2V_{pp}$ at 1 KHz and observe the output waveform.
3. Measure and record output waveform.
4. Verify your result using PSPICE.

![Figure 3.6 Voltage Doubler](image)

Question

1. What changes would you do to the circuit of figure 3.6 to build a simple clamping circuit? What would the output look like? Verify your design and output using PSPICE.
LAB 4
OPERATIONAL AMPLIFIER

The purpose of this lab is to learn the basic Operational Amplifier (op-amp) characteristics.

Concept

A typical op-amp is an 8 pin integrated circuit that has a direct coupled, high gain differential amplifier. The input stage of op-amp is a differential amplifier with two inputs, non-inverting input marked with (+) symbol and inverting input marked with (−) symbol. An op-amp is designed to sense the difference between the voltage signals applied at its two input terminals. The output stage of op-amp is designed to provide the required output voltage swing and the required output current. Figure 4.1 shows the pin configuration of 741 Op-Amp IC and its symbol.

Thus, if we provide input voltages \( V_{in}^{+} \) and \( V_{in}^{-} \) at the two input terminals of an op-amp, whose open loop gain is \( A \), then its output voltage will be \( V_{out} = A (V_{in}^{+} - V_{in}^{-}) \). Hence, if \( V_{in}^{+} = V_{in}^{-} = 0 \text{ V} \) then \( V_{out} = 0 \text{ V} \).

But due to imperfections, there may be a non-zero output voltage even when both input terminals are connected to ground. This non-zero output voltage is referred to the input voltage is called the offset voltage, \( V_{os} \) given by

\[
V_{os} = \frac{V_{out}}{A_{v}}
\]

where \( A_{v} \) is the closed loop voltage gain

and \( V_{out} \) is the output voltage when both inputs are connected to ground.

If the input signal is very large the op-amp output typically saturates within few tenth to 1 V of the positive and the negative power supplies. The output voltage gets clipped-off beyond these voltage saturation levels. Thus, the maximum undistorted output swing possible is always less than \( (V^{+} - V^{-}) \).

The change in the output voltage is limited by maximum rate of change possible at the output, thus , preventing the output signal to respond immediately to high frequency signals. This maximum rate of change is called the Slew Rate (SR) and is given by

\[
SR = \left. \frac{dv_{out}}{dt} \right|_{max}
\]
Experiment

- Use IC LM741 op-amp.
- Always make sure that the pin numbers are correctly identified.
- The values of the power supply voltages are usually 12 V to 15 V each (both positive and negative supply voltages).
- Make sure that the positive and the negative input voltages are connected to pin numbers 7 and 4, respectively.
- Pin number 8 is always NOT connected (NC) to anything.

![Figure 4.2a Circuit for Input Offset Voltage](image)

![Figure 4.2b Offset Voltage nullifying](image)

**PART A - Input Offset Voltage**

1. Build the circuit as shown in Figure 4.2a
2. Measure the output voltage.
3. Calculate input offset-voltage using the following formula
   \[ V_{os} = \frac{V_{out}}{A_v} \]
   where \( A_v = 1 + \frac{R_F}{R_1} \)
4. Compare your calculated \( V_{os} \) with data sheet. Show the comparison in tabular form.
5. Now build the circuit as shown in Figure 4.2b
6. Observe \( V_{out} \) and vary \( R_{var} \) until \( V_{out} = 0 \) V.
7. Measure \( R_{var} \).

**PART B - Output Voltage Swing**

1. Build the circuit as shown in figure 4.3
2. Apply \( V_{in}^- = 1 \) Vpp at 1KHz and vary \( V^+ \) and \( V^- \) from 12 V to 15 V in steps of 1 V such that \( V^+ = |V^-| \)
3. Record the output waveform for each supply voltage value.
4. Also calculate and draw expected output waveforms.
5. Fix \( V^+ \) and \( V^- \) at 12 V and -12 V, respectively, \( R_F \) at 47 K and \( R_1 \) at 10 K. Vary the input voltage from 1 V to 3 V at 1 KHz and record the output voltage waveforms.
6. For each case record what the maximum output voltage swing before the output gets saturated.
7. Verify your result with PSPICE.
PART C - Slew Rate

1. Build the circuit as shown in figure 4.4
2. Apply $V_{in}^+ = 1V_{pp}$ square waveform at 1 KHz.
3. Observe output signal and calculate slew rate.
4. Compare your slew rate with data sheet. Show your comparison in a tabular form.

PART D - Frequency Response

1. Build the circuit as shown in figure 4.5
2. Apply $V_{in}^+ = 1V_{pp}$ at 1 KHz.
3. Vary frequency from 100 Hz to 3 MHz and measure $V_{out-pp}$. Record your measurement in tabular form.
4. Plot logarithmic graph for frequency response. 3dB point should be clearly marked.
5. What is your bandwidth? Compare bandwidth calculated from the experimental plot with the data sheet value.
LAB 5
BASIC OP-AMP CIRCUIT

In this lab you will examine comparator, Schmitt trigger and effects of hysteresis.

Concept

One of the basic applications of op-amp is a comparator. A comparator compares voltage levels between an applied voltage and reference voltage. Figure 5.1 shows a comparator where input $V_{in}^-$ is grounded and other input $V_{in}^+$ is connected to a varying dc voltage. When $V_{in}^+ < V_{in}^-$ the output voltage $V_{out}$ is at $-V_{sat}$ (see figure 5.1b). On the other hand when input $V_{in}^+ > V_{in}^-$, $V_{out}$ is $+V_{sat}$. Thus, $V_{out}$ changes from one saturation level to another whenever $V_{in}^+ = V_{in}^-$. 

Another application of op-amp is Schmitt trigger. Figure 5.2 shows a Schmitt trigger circuit. In this $V_{in}^-$ triggers $V_{out}$ everytime it exceeds certain voltage levels called upper threshold voltage, $V_{ut}$ and lower threshold voltage, $V_{lt}$ as shown in figure 5.3. As long as $V_{in}^+ < V_{ut}$, $V_{out}$ is at $+V_{sat}$ and when $V_{in}^+ > V_{ut}$, $V_{out}$ is at $-V_{sat}$.

The $V_{ut}$ and the $V_{lt}$, are given by the following equations

$$V_{ut} = \frac{R_1}{R_1 + R_2}(+V_{sat})$$

$$V_{lt} = \frac{R_1}{R_1 + R_2}(-V_{sat})$$

Figure 5.1 (a) Conceptual comparator diagram (b) Transfer Characteristics curve of a comparator
Figure 5.2 Schmitt Trigger

Figure 5.3 Input and Output waveform of Schmitt trigger
Experiment

![Comparator diagram](image)

**Figure 5.4 Comparator**

**PART A-Comparator**

1. Build the circuit as shown in Figure 5.4
2. Apply $V_{in}^- = 0$ V and vary $V_{in}^+$ from -5 V to +5 V dc in steps of 0.5 V (non-inverting configuration).
3. Measure $V_{out}$ for each $V_{in}^+$.
4. Now vary $V_{in}^+$ from 5 V to -5 V dc in steps of 0.5 V and measure $V_{out}$ for each $V_{in}^+$.
5. Plot $V_{out} \text{ vs } V_{in}^+$ for both the cases on the same graph.
6. Record the saturation voltage levels.
7. Now apply $V_{in}^- = 1$ V and repeat step 2 to step 6.
8. Verify your observation using PSPICE.

**PART B-Schmitt Trigger**

1. Build the circuit as shown in Figure 5.2
2. Apply $V_{in}^+ = 1 V_{pp}$ at 1 KHz
3. Record your input and output waveform.
4. Extrapolate $V_{ut}$ and $V_{lt}$ from the recorded waveforms and compare them with the theoretical values.
5. Verify your observation with PSPICE.

**Questions**

1. Design a triangular waveform generator using a bistable comparator and an integrator. Submit all your PSPICE work.
LAB 6
MOSFET CHARACTERIZATION

The purpose of this lab is to understand the current-voltage characteristics of a n-channel MOSFET (i.e. to understand the dependence of drain current on gate voltage and drain-source voltage).

Concept

MOSFET is a four-terminal device with the terminals named as Source, Gate, Drain and Substrate (or Body). In a n-channel MOSFET, the substrate (which is p-type) is connected to ground or a negative voltage. Source and drain are two heavily doped regions with carrier type opposite to that of the substrate (p-type). Gate region is in between source and drain and is stacked with an oxide layer and a metal layer over it. Schematic of an n-channel MOSFET is shown in Figure 6.1.

In NMOS transistor, a positive voltage is applied to the gate terminal to create a n-channel underneath the gate and thus, forming a conductive region from the source to the drain.

When a drain-source voltage is applied to the NMOS transistor, carriers (electrons) flow from the source region to the drain region through the channel created underneath the gate. This flow of current, called the drain current, \( I_D \), depends on the gate voltage \( V_G \), drain-source Voltage \( V_{DS} \), threshold voltage \( V_T \) and various physical parameters \( k_n \).

In triode region, when the applied \( V_{DS} < (V_G - V_T) \), the drain current shows linear dependence on \( V_{DS} \) and is given by

\[
I_{D\text{-lin}} = k_n \left[ (V_G - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]
\]

When the applied \( V_{DS} \geq (V_G - V_T) \), the drain current reaches a saturation and is given by

\[
I_{D\text{-sat}} = \frac{1}{2} k_n (V_G - V_T)^2
\]

Figure 6.1 (a) cross-sectional view of a n-channel MOSFET (b) Circuit symbol of n-channel MOSFET
Experiment

Use N-Channel MOSFET – ZVN2110A

![Circuit Diagram](image)

Figure 6.2 Circuit for MOSFET Characteristics

**PART A** $i_D$ vs $V_{DS}$ characteristics

1. Build the circuit as shown in Figure 6.2
2. Vary $V_{GS}$ (by varying $V_{GG}$) from 0 V to 3 V in steps of 0.5 V and for each $V_{GS}$ vary $V_{DS}$ (by changing $R$ and $V_{dd}$) from 0 V to 10 V in steps of 0.2 V until reaching close to saturation and steps of 1 V latter. Measure $I_D$ at each $V_{GS}$ and $V_{DS}$ step.
3. Plot $I_D$ vs $V_{DS}$ for each $V_{GS}$ on the same graph.
4. Label the triode region and the saturation region on the plot.
5. Calculate $i_D$ using the formulae given in previous page and plot theoretical $i_D$ vs $V_{DS}$ graph for step 2.
6. Compare your measured data, theoretical data and verify using PSPICE.

**PART B** $I_D$ vs $V_{GS}$ characteristic

1. Build the circuit as shown in Figure 6.2
2. Vary $V_{GS}$ from 0 V to 5 V in steps of 1 V and measure $I_D$ for a fixed $V_{DS} = 10$ V.
3. Plot $I_D$ vs $V_{GS}$ graph.
4. Calculate $i_D$ using the saturation current formula and plot theoretical $I_D$ vs $V_{GS}$ on the same axes as in step 3.
5. Determine the theoretical and experimental transconductance from the graphs plotted in step 3 and step 4 and compare the values with the data sheet value.
6. Compare your results in Step 4 and Step 5 using PSPICE results.
PART C – Voltage Transfer Characteristic

1. Build the circuit as shown in Figure 6.2
2. Vary $V_{GS}$ from 0 V to 5 V in steps of 0.5 V and measure $V_{DS}$ for each case. Decrease the steps voltage in the region where $V_{DS}$ is very sensitive to $V_{GS}$.
3. Plot Voltage Transfer Characteristic curve.
4. Determine $V_t$ from the plot and compare with datasheet value.
5. Verify your plot using PSPICE.

QUESTIONS

1. Draw the biasing circuit of a p-channel MOSFET and show the directions of transistor terminal currents in the diagram.
The goal of this lab is to examine various types of basic MOSFET amplifier configurations and characterizing them.

**Concept**

There are three basic configurations of MOSFET amplifier. Each configuration is obtained by connecting one of the three terminals (Source, Gate and Drain) to ground and making it common to both input and output ports. Thus, we can have common-source (CS) amplifier, common-gate (CG) amplifier and common-drain (CD) amplifier. The CD amplifier is also known as Source-follower.

Characterization of amplifiers include determining input resistance, $R_{in}$; open-circuit ($R_L = \infty$) voltage gain, $A_{vo}$; output resistance, $R_o$; closed-circuit (finite $R_L$) voltage gain, $A_v$; and overall voltage gain, $G_v$. See figure 7.1

![Figure 7.1 Characterization of an MOSFET amplifier](image)

$R_{in}$ represents the loading effect of the amplifier on the signal source. $V_i$ become almost equal to $V_{sig}$ if $R_{in}$ is far far greater than $R_{sig}$. $R_{in}$ is given by

$$R_{in} = \frac{V_i}{I_i}$$

$A_{vo}$ represents the voltage gain with no load. It is given by

$$A_{vo} = \frac{V_o}{V_i} \bigg|_{R_L = \infty}$$

$R_o$ represents the resistance looking back into the output terminal. To determine $R_o$, we first measure output voltage without connecting load $R_L$. Then we connect a variable load across the output port and vary the load $R_L$ until the output voltage is equal to one-half of the open circuit value. The $R_L$ value at this point is the output resistance of the amplifier.
$A_v$ represents the voltage gain with a finite load. It is given by

$$A_v = \frac{V_o}{V_i}$$

$G_v$ represents the overall voltage gain and it is given by

$$G_v = \frac{V_o}{V_{sig}} = \frac{V_o}{V_i} \times \frac{V_i}{V_{sig}}$$

**Experiment**

![Figure 7.2 CS Amplifier with a bypassed $R_s$](image1)

![Figure 7.3 CS amplifier with an un-bypassed $R_s$](image2)

**PART A - Common Source Amplifier**

1. Design and build the common source amplifier as shown in figure 7.2 such that the Q-point of the MOSFET is at $I_D = 5$ mA and $V_{DS} = 5$ V; $V_G = 7.5$ V and $(R1 + R2) = 200$ KΩ.
2. Provide $V_{sig} = 200$ mV$pp$ at 5 KHz frequency and measure the output voltage.
3. Record pictures of the input and output waveforms and calculate the gain.
4. Vary $V_{sig}$ and determine the maximum peak-to-peak output voltage without distortion. In each case, note the corresponding $V_{sig}$.
5. Measure input resistance and output resistance. (See conceptual section for steps to measure them).
6. Fix $V_{sig}$ at a value that does not produce a non-linear (distorted) output signal. Vary the input signal frequency and measure the output voltage at each frequency. Plot frequency response on a graph paper and determine the amplifier bandwidth.
7. Compare your results with hand calculations and PSPICE results. Show your comparison in a tabular form.

**PART B – Common Source Amplifier with an un-bypassed Source Resistance**

1. Build the circuit shown in figure 7.3
2. Repeat Step 2 to Step 7 of Part-A.
3. Compare gain, $R_{in}$, $R_o$ and bandwidth of the amplifier with that of PART A.
PART C - Common Gate Amplifier

1. Build the circuit as shown in figure 7.4
2. Repeat Step 2 to Step 7 of Part-A.

PART D - Common Drain Amplifier

1. Build the circuit as shown in figure 7.5
2. Repeat step 2 to step 7 of Part-A.

**Question**

1. Design a CS amplifier using active bias and active load for a bias current of 1 mA and a gain of > 1000. Verify your design using PSPICE.
LAB 8
BJT CHARACTERISTICS

The purpose of this lab is to understand the characteristics of a npn BJT i.e. to understand the current-voltage relationships and design parameter dependencies.

Concept

Bipolar junction transistor (BJT) is a three terminal device with the terminals named as emitter (E), base (B) and collector(C). In a npn-BJT, the emitter and the collector regions are of n-type while the central base region is of p-type. In this device, the terminal currents are mainly dependent on the base-emitter voltage, $v_{BE}$, and to a lesser extent on the base-collector voltage, $v_{CB}$. The structure of the device and the circuit symbol are shown in Figure 8.1.

BJT consists of two pn junctions, the emitter-base junction and collector-base junction. Depending on the bias condition of each of these junctions, current flows across the junctions accordingly. Current-Voltage equations are as given below.

\[
i_C = I_s \exp\left(\frac{v_{BE}}{\beta}\right)
\]
\[
i_B = \frac{i_C}{\beta}
\]
\[
i_E = \frac{i_C}{\alpha}
\]
\[
i_E = i_C + i_B
\]

where

- $i_C, i_B, i_E$ are collector, base and emitter current, respectively.
- $I_s$ is saturation current, also known as scaling current.
- $v_{BE}$ is voltage across base-emitter junction
- $\alpha, \beta$ are transistor parameters called common-base current gain and common-emitter current gain, respectively.

A DC voltage source is needed to place the BJT in the active region (base-emitter junction forward bias and base-collector junction reverse bias) to use it as an amplifier. The BJT amplifier design involves both DC operating point ($I_C, V_{CE}$) design and the AC performance (voltage gain, input resistance and output resistance) design.

Figure 8.1 a) Cross-sectional schematic of npn BJT (b) Circuit symbol of npn BJT
Experiment

Figure 8.2 Circuit used for measuring current-voltage characteristics

Use npn-BJT – 2N2222

PART A - BJT Terminals Identification

1. Identify the terminals of the BJT. Draw a schematic showing the terminals of the BJT and describe how you identified the terminals.
2. From the data sheet note down the values of $\alpha$, $\beta$, $I_s$, and $g_m$.

PART B - $i_C$ vs $v_{CE}$ characteristics

1. Build the circuit as shown in Figure 8.2
2. Vary $i_B$ (by varying $V_{bb}$) from 0 to 25 uA in steps of 5 uA and for each $i_B$ value vary $v_{CE}$ (by varying R and $V_{CC}$) from 0 V to 10 V first in steps of about 0.2 V until the current nearly saturates and then steps of 1 V. Measure $i_C$ for each $v_{CE}$ and $i_B$ values.
3. Plot $i_C$ vs $v_{CE}$ for all $I_B$ values on the same graph.
4. Label the active region and the saturation region on the plot.
5. Using the formulae calculate the values of $\alpha$, $\beta$ and $I_s$ from the data recorded in step 2 and compare them with the data sheet values. Obtain $\alpha$ value as $\frac{\beta}{1+\beta}$.
6. Verify your $i_C$ vs $v_{CE}$ plot using PSPICE.

PART C - $i_C$ vs $v_{BE}$ characteristics

1. Build the circuit as show in Figure 8.2
2. Vary $v_{BE}$ from 0 V to a maximum voltage that can be reached in steps of 0.1 V and measure $i_C$ for each $v_{BE}$ value.
3. Plot $i_C$ vs $v_{BE}$ graph.
4. Determine transconductance, $g_m$, from the graph plotted in Step 3 and compare it with the value in the data sheet.
5. Compare and verify your results in step 3 and step 4 using PSPICE.

QUESTIONS

2. Draw the biasing circuit of a pnp transistor and show the directions of the transistor terminal currents in the diagram.
LAB 9
BASIC BJT AMPLIFIER

The purpose of this lab is to study the basic BJT amplifier configurations and understand their characteristics.

Concept

There are three basic configurations of a BJT amplifier. Each configuration is obtained by connecting one of the three terminals (Emitter, Base and Collector) to ground and making it common to both input and output ports. Thus, we can have common-emitter (CE) amplifier, common-base (CB) amplifier and common-collector (CC) amplifier. The CC amplifier is also known as Emitter-follower.

Characterization of amplifiers include determining their input resistance, $R_{in}$; open-circuit voltage gain ($R_L = \infty$) $A_{vo}$; output resistance, $R_o$; closed-circuit voltage gain (finite $R_L$), $A_v$; and overall voltage gain, $G_v$. See figure 9.1

$R_{in}$ represents loading effect of the amplifier on the signal source and together with $R_{sig}$ it reduces the voltage $V_{sig}$ to $V_i$ at the amplifier input, $V_i = V_{sig} \times \frac{R_{in}}{R_{in}+R_{sig}}$. $R_{in}$ is given by

$$R_{in} = \frac{V_i}{i_i}$$

$A_{vo}$ represents voltage gain with no load. It is given by

$$A_{vo} = \frac{V_o}{V_i} \bigg|_{R_L = \infty}$$

$R_o$ represents the resistance looking back into the output terminal. It is determined in the same way as explained in Lab 7.

$A_v$ represents voltage gain with finite $R_l$. It is given by

$$A_v = \frac{V_o}{V_i}$$

$G_v$ represents overall voltage gain and is given by

$$G_v = \frac{V_o}{V_{sig}} = \frac{V_o}{V_i} \times \frac{V_i}{V_{sig}}$$

Figure 9.1 Characterization of the BJT amplifier
Experiment

PART A - Common Emitter Amplifier

1. Design the common emitter amplifier as shown in figure 9.2 such that Q-point of the transistor is at $V_{ce} = 7.5$ V and $I_c = 0.75$ mA, $V_B = 2.25$ V and $(R_1 + R_2) = 26$ KΩ.
2. Provide $V_{sig} = 200$ mVpp at 5 KHz frequency and measure output voltage.
3. Record pictures of the input and output waveforms and calculate the gain.
4. Vary $V_{sig}$ to find the maximum peak-to-peak output voltage without distortion. Record the corresponding $V_{sig}$.
5. Measure input resistance and output resistance as explained in Lab 7.
6. Fix $V_{sig}$ at a value that does not produce a non-linear (distorted) output signal. Vary the input signal frequency and measure the output voltage at each frequency. Plot frequency response on a graph paper and determine the amplifier bandwidth.
7. Compare your results with hand calculations and PSPICE results. Show your comparison in a tabular form.

PART B – Common Emitter Amplifier with Emitter Resistance

1. Modify the circuit of Part-A as shown in figure 9.3
2. Repeat Step 2 to Step 7 of Part-A.
3. Compare gain, $R_{in}$, $R_o$ and bandwidth of the amplifier with that of PART-A.

PART C - Common Base Amplifier

1. Build the circuit as shown in figure 9.4
2. Repeat Step 2 to Step 7 of Part-A.
PART D - Common Collector Amplifier

1. Build the circuit as shown in figure 9.5
2. Repeat step 2 to step 7 of Part-A

![Figure 9.4 Common Base Amplifier](image)

![Figure 9.5 Common Collector Amplifier](image)

Question

2. Design and build a CE amplifier using active bias and active load for a bias current of 1mA and a gain > 100. Verify your design using PSPICE.
LAB 10
AUDIO POWER OPERATIONAL AMPLIFIER

In this lab you learn about the Audio Power Operational Amplifier

Concept

In this lab, you are introduced to a device called a piezoelectric element. The piezoelectric element is made from a certain crystalline or ceramic substance which acts as a transducer at audio frequencies. When subjected to mechanical stress, the piezoelectric element will produce an electric potential. When subjected to an electric voltage, the element will vibrate.

Another component you will use in this lab is an audio power operational amplifier, LM386. It is a low voltage audio power amplifier which is used in many commercial products for amplifying low level signals to a level that can be heard by human ears.

The supply voltage for the LM386 can range from 4 V\textsubscript{DC} to 12 V\textsubscript{DC}. The voltage gain can vary from 20 to 200. Please refer to the data sheet for other specifications. These devices are used as microphones, sensors for car alarms, earphones or any general purpose alarms.

![Figure 10.1 Pin Configuration of LM386](image)

**Figure 10.1 Pin Configuration of LM386**

Experiment

![Figure 10.2 X20 Amplifier Circuit](image)

**Figure 10.2 X20 Amplifier Circuit**
PART A – Piezoelectric Element

1. Connect one end of the oscilloscope probe to one terminal of the piezoelectric element and the other end of the oscilloscope probe to the other terminal of the piezoelectric element. It does not matter which wire from the element is connected to the oscilloscope probe end.
2. Set the voltage scale on one channel of the scope to the 50 mV range. Set the time base to about 20 ms. Tap on the element with your finger while observing the scope. Record what happens.
3. Change the voltage scale on the scope to 10 mV and the time base to 2 ms. Now talk into the element, changing the frequency and the level of your voice while observing the scope. Record what happens.
4. Now connect the element to the speaker (either wire from the speaker can be connected to either wire of the element). Tap, talk and whistle into the element and record what happens.

PART B – X20 Amplifier Circuit

1. Build the X20 amplifier circuit as shown in figure 10.2
2. Double check the wiring of your circuit. Turn the power ON.
3. Try tapping on, talking and blowing air into the element. Did you hear any amplification?
4. Measure $V_{in-pp}$ while talking and blowing air into the piezoelectric element.
5. Measure $V_{out-pp}$ while talking into the element (try to keep your voice level same as before and try to blow air with same intensity and speed). Record the level.
6. What is your gain?

PART C – X200 Amplifier Circuit

1. Build the circuit as shown in figure 10.3
2. Double check the wiring of your circuit. Turn the power ON.
3. While blowing air into the element vary R1 until you hear some noise from the speaker.
4. Repeat step 3 to step 6 of Part A.
PART D – Audio Frequency Oscillator

1. Build the circuit as shown in figure 10.4. Use C equal to 0.068μF.
2. Turn the power ON.
3. What do you hear from the speaker?
4. Measure $V_{out/pp}$.
5. Change C to 1μF, 10μF, 47μF and 100μF and measure $V_{out/pp}$ for each case.
6. Record your observation for each value of C.

Figure 10.4 Audio Frequency Oscillator