Tutorial on
Troubleshooting and Data Analysis
Using Intronix Logicport 34-Channel Logic Analyzer

ver. 1.0
1. **Experiment Description:**

The test bed for this tutorial is a simple PicoBlaze system, including PicoBlaze, 1k x 18 instruction ROM, and external 64 x 8 bit RAM with addresses 0x00-0x3F. The program reads bytes from locations 0x00-0x1F, adds 0x20 to each of them, and writes modified data to locations 0x20-0x3F.

Nexys3 board is connected to logic analyzer through the 16 POD connector, using UCF file. Following are the signals that are interfaced between Nexys3 board and logic analyzer.

1. 8 bits of data bus
2. 6 bits of address bus
3. 1 bit of write enable
4. 1 bit of clock

The analyzer will display the contents of data bus, address bus and write enable in each clock cycle.
2. **Intronix Logicport 34 Channel Logic Analyzer:**

Link to install LogicPort software on your computer

http://www.pctestinstruments.com/downloads.htm

**Introduction:**

The logic analyzer has

- 38 total wires
- 34 data channels (rainbow wires)
- 2 clock channels (white wires)
- 4 ground channels (grey wires)
- Up to 500MHz sampling rate
- Input impedance: 200K ohms
- The box holds an FPGA which does all of the sampling
Data and Clock Channels:

The logic analyzer has 32 data channels. The grey and white wires are not data wires. The wire colors and tip colors match with the wire ID colors displayed in the software. For example, Brown wire with a white tip is D1 (the brown letters with white background).

There are two clock channels (white wires, CLK1, CLK2)

**Interface Nexys3 board to Logic analyzer using 16-pin POD connector:**

Connect all 16 pins (data bus, address bus, wr_en and clock) of Nexys3 board to the POD connector.
**Software Toolbar:**

Software toolbar can be used to do

1. Measurement setup
2. Sample Mode setup
3. Trigger setup
3. Design Flow:

In order to analyze and view data on the logic analyzer, there are five major steps involved.

1. Setting up an Acquisition
   i. Creating a new file
   ii. Adding signals
   iii. Creating Groups
   iv. Group settings (format, order, analogue/digital/color)

2. Sample mode setup
3. Triggering condition
4. Sample rate
5. Logic threshold
6. Run

1. Setting up an Acquisition:

Creating a new file:

Create a new file to keep all of your settings in the end. You can later reload the pre-existing setup file to run the same measurement.

Remove the standard Group (Data[31..0]) and the clock signals initially, so you can add the signals required for your design only.

Adding signals and Creating groups:

Signals and group of wires can be added or taken away by right clicking the area below the signals.

To remove the signals or groups, right click the signal and select “Remove group”.

Default groups are 8-bit, 16-bit and 32-bit groups, starting from the Data0 signal and going upwards. You can create your own group (for example, a 6-bit bus) by clicking “Add Group->Create button”
Rename the group using “Edit group” option.

Select the appropriate group that you want to include into your design.

Groups are useful when looking at parallel data buses because the software will interpret the data for you. Rename the signals using “Edit Signal” option that are group into Data Bus and Addr group.
The overall set of signals include two groups “Data” and “Addr”. Data group is 8 signals whereas Addr group has a set of 6 signals. The other two signals include clock and write enable.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Wire ID</th>
<th>Wire Status</th>
<th>Edge A</th>
<th>Cursor A</th>
</tr>
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<tbody>
<tr>
<td>Data</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data0</td>
<td>D0</td>
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<td>1</td>
<td>c</td>
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<td>Data1</td>
<td>D1</td>
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<td>D4</td>
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<tr>
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<td>D5</td>
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</tr>
<tr>
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<td>D6</td>
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</tr>
<tr>
<td>Data7</td>
<td>D7</td>
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<td>Addr</td>
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<td>Addr 5</td>
<td>D13</td>
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<td>2h</td>
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<td>Addr 1</td>
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<td>Addr 0</td>
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<td>clk</td>
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<td></td>
</tr>
<tr>
<td>wr_en</td>
<td>D15</td>
<td>L</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
Group settings:

Right click on any group to edit group settings. The following options are available:

- Format: Can be binary, hex or decimal
- Order: To decide which bit is displayed at the top of the group
- Style: Interpret the bits as analogue value.
- Color: To change colors

2. Sample Mode setup:

Can be configured to two different modes

Timing Mode: Use the internal clock, sampling rate is chosen using the sample rate drop down menu on the main screen.

Sampling is driven by an internal clock (100kHz -> 100K samples per second)

State Mode: Sampling is driven by user defined settings and an external signal. The signal can only be from the CLK1 wire or the CLK2 wire.
3. **Sample rate:**

The sampling rate is selected (when in timing mode) with the use of the drop down box.

4. **Logic threshold:**

The logic threshold determines where the analyzer will detect a high (binary 1) and where it will detect a low (binary 0).

5. **Triggering condition:**

The trigger determines when the buffer is sent to the computer.

Specify only condition A to detect an edge of the signal.
When the user presses the button, RAM address is incremented and RAM write enable is HIGH. RAM write enable is used as a trigger signal.

Click on the icon highlighted in RED for a single acquisition of the data.

Program waits for the user to enter the button.
As soon as trigger is generated, the tool populates the updated waveform on the screen.

Use the print option to save the waveform in the PDF format.