ECE 448, FPGA and ASIC Design with VHDL
Spring 2017

Instructor

Dr. Jens-Peter Kaps
The Nguyen Engineering Building, room 3224
Office hours: Monday 3:30-4:30 PM, Tuesday 1:30-2:30 PM, and by appointment

Lecture

Monday, Wednesday 1:30-2:45 PM, Blue Ridge Hall, room 129

Web page

everything will be posted on myMason

Grading

Lab assignments: 40% + 2% bonus
Midterm exam for the lecture: 10%
Midterm exam for the lab: 15%
Quizzes & homework: 10%
Final exam: 25%

Schedule (subject to possible modifications):

1. Objectives, Scope, and Organization. 01/23
2. VHDL Refresher. 01/25
3. Combinational-Circuit Building Blocks. 01/30, 02/01
4. Sequential-Circuit Building Blocks. 02/06
5. FPGA Devices and FPGA Design Flow. 02/08
6. Finite State Machines: State Diagrams, State Tables, ASM Charts, and VHDL Code. 02/15, 02/20
7. Modeling of Circuits with a Regular Structure. 02/22
8. Review before the Midterm Exam. 02/27
9. Midterm Exam. 03/01
10. VGA Display – Graphics. 03/06, 03/08
11. VGA Display – Animation and Text. 03/20, 03/22
12. Xilinx FPGA Memories. 03/27, 03/29
13. Design Methodology. 04/03, 04/05
14. PicoBlaze Overview. 04/10
15. PicoBlaze I/O and Interrupt Interface. 04/12
16. PicoBlaze Programming and Instruction Set. 04/17, 04/19
17. Trends in Modern FPGAs. FPGAs vs. ASICs. 04/24, 04/26
18. Review before the Final Exam. 05/01
   **Final Exam. 05/10, 1:30-4:15pm**

**Literature**

**Required Textbooks**


**Supplementary Textbooks**


**Honor Code**

All rules of the Mason Honor Code will be strictly enforced. You should review the rules and interpretations of the Mason Code available at [http://oai.gmu.edu/the-mason-honor-code](http://oai.gmu.edu/the-mason-honor-code), and be familiar with them.

**Students with Disabilities**

If you need special assistance, please inform the instructor and the Office of Disability Services (ODS, [http://ods.gmu.edu](http://ods.gmu.edu)) as soon as possible. All special accommodations must be arranged through ODS.