George Mason University
Volgenau School of Engineering
Department of Electrical and Computer Engineering

ECE 511: Microprocessors
Syllabus
Fall 2018

Professor: Avesta Sasan

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Lecture: Wednesdays @ 4:30om – 7:20 PM @ Blueridge Hall 129

Office Hours: Thursdays 4:00-5:00pm

Prerequisites: A computer architecture course equivalent to ECE445 @ GMU
Ability to program using C/C++

Required Text: *No textbook is required.*

Recommended Text: *Computer Organization and Design, 5th Edition*, by Hennessey and Patterson.
ISBN-13: 978-0-12-407726-3

Course Webpages: https://mymasonportal.gmu.edu/ (**Blackboard**)

Textbook Website: http://textbooks.elsevier.com/9780124077263

Who can take the course (Restrictions):

Must be enrolled in one of the following Levels:
- *Graduate*
- *Non-Degree*
- *Undergraduate*

May not be enrolled in one of the following Degrees:
- *Non-Degree Undergraduate*

Must be enrolled in one of the following Colleges:
- *Schar School of Policy and Gov*
- *College of Science*
- *Volgenau School of Engineering*

May not be enrolled in one of the following Campuses:
- *GMU Korea*

Must be enrolled in one of the following Classifications:
- *Advanced to Candidacy*
- *Graduate*
- *Non-Degree*
- *Senior Plus*

COURSE DESCRIPTION (FROM GMU COURSE CATALOG)

Introduces microprocessor software and hardware architecture. Includes fundamentals of microprocessor system integration, instruction set design, programming memory interfacing, input/output, direct memory access, interrupt interfacing, and microprocessor architecture evolution. Studies Intel family of microprocessors, and reviews other microprocessor families and design trends. Offered by Electrical & Comp. Engineering. May not be repeated for credit.

LEARNING OUTCOMES

Following successful completion of ECE 511, the student will be able to:

1. Explain how single cycle and multi-cycle MIPS architecture work.
2. Explain how MIPS superscalar are constructed and how they work.
3. Explain the difference between in-order and out-of-order execution.
4. Explain dynamic scheduling and be able to execute score-boarding and Tomasulo's algorithms.
5. Identify pipeline hazards and how explain how register renaming resolve these hazards.
6. Explain problems and solutions related to keeping precise state during the execution of a program.
7. Explain the difference between loosely coupled and tightly coupled microprocessors
8. Be able to apply Amdahl's law to multi-core processors.
9. Identity and explain the bottlenecks related to parallel processing
10. Be able to explain the difference between symmetric and asymmetric multicore processors
11. Explain how asymmetry could be used for energy efficiency in multicore systems.
12. Explain the memory consistency problem and related solutions in multi-processor systems.
13. Be able to explain the sequential consistency in multi-processor systems, understand related issues and explain the related solutions.
14. Be able to explain the problem of cache coherence in multi-processor and multi-core systems,
15. Explain the coherency solutions and execute the related algorithms.
16. Be able to understand and execute various cache coherency solutions including MSI, MESI, Directory based, etc.
17. Understand different types of interconnects used in multi-processor solutions.
18. Explain how Network-on-Chip solutions are constructed, and how info. packets travel in NoCs.
19. Explain the different between fine-grain and simultaneous multithreading.
20. Explain the changes to be made to a pipeline processor to support multithreading.

SCHEDULE

Tentative Schedule* subject to change *

1. Introduction (Week 1)
2. **Review*** of Single Cycle MIPS (Week 2)
3. **Review*** of Pipelined MIPS (Week 3)
4. Additional background (Week 4)
5. Pipelining, Concept of Superscalar (Week 5)
6. Superscalar Processors (Week 6)
7. Multicores Processors (Week 7)
8. **Midterm** (Week 8)
9. Advanced Cache Management (Week 9)
10. Speculation (Week 10)
11. Emerging Memory technologies (Week 11)
12. Multi-Threading (Week 12)
13. Interconnect and NoCs (Week 13)
14. SIMD and GPU (Optional if we had time)
15. **Final** (Week 14)

CLASS MEETINGS

According to the literature cited in the Association for the Study of Higher Education (ASHE) report, in order for students to learn they must do more than just listen: they must read, write, discuss, or be engaged in solving problems. In particular, students must engage in such higher-order thinking tasks as analysis, synthesis, and evaluation. Active learning engages students in two aspects – doing things and thinking about the things they are doing. [Wikipedia: Active Learning]

Active learning is the process whereby students engage in activities, such as reading, writing, discussion, or problem solving, that promote analysis, synthesis, and evaluation of class content. [University of Michigan – Center for Research on Learning and Teaching. http://www.crlt.umich.edu/tstrategies/tsal]

ASSIGNMENTS

You are required to read the assigned papers, and write a 1 page summary for each paper.
The paper summaries should be prepared in IEEE format (single page, double column). Details required for preparing the paper summaries will be covered in detail in one of the lectures. Assigned papers are key papers in computer architecture.

Paper summaries should be submitted by 11:59 PM on the specified due date.
Late submission will NOT be accepted.
Cheating on a reading assignment (copying someone else's work, even partially) will result in a zero (0) for that assignment.

EXAMS

This course includes **a Midterms** exam and **a Final exam**. Exam dates are specified in the course schedule.

Each exam will consist of: (1) a set of multiple-choice questions; and (2) several long-answer questions. You **will not need Scantron** form for answering the multiple-choice portion of each exam.

All exams are **cumulative**.

All exams are **closed book**. You will be allowed to use the MIPS Reference card on all exams. I will provide additional reference materials and scrap paper, as needed.

If (for extraordinary circumstances) you cannot make one of the scheduled exams, you must speak with me **in advance** to arrange for an alternate time to take the exam.

If you fail one of the exams or do not submit paper summaries, I reserve the right to give you a failing grade for the course.

ATTENDANCE

Attendance in the class is mandatory. If you miss class you must consult with one of your classmates to obtain the notes and/or problem solutions that were presented.

COURSE GRADE

The final grade for the course is based on my best assessment of your understanding of the material and your participation in the class during the semester. The exams, labs, homework assignments, and class problems will be used to determine your final grade according to the following weighting:

Paper summaries	20%
Attendance	10%
Midterm Exam	30%
Final Exam	40%

The final letter grade will be assigned accordingly.

Please note that you are responsible for making sure that all of your grades are posted on Blackboard and that they are correct. If you wish to challenge a grade you must do so **within two weeks** of it being posted on Blackboard. Grades will not be changed more than two weeks after they were posted.

ACADEMIC INTEGRITY

The George Mason University Honor Code is stated as follows:

"*To promote a stronger sense of mutual responsibility, respect, trust, and fairness among all members of the George Mason University community and with the desire for greater academic and personal achievement, we, the student members of the University Community have set for this:*

Student members of the George Mason University community pledge not to cheat, plagiarize, steal, and/or lie in matters related to academic work."

You are expected to abide by the Mason Honor Code. Violations of the Honor Code are taken very seiously and will be prosecuted to the fullest extent. This includes, but is not limited to, cheating on homework assignments, quizzes, projects, labs, and exams.

As indicated above, you are encouraged to work together on assessments, and share ideas about solutions to problems. However, you must submit your own work. Copy the solution from another student, or from the author's solution manual, is considered cheating and is a violation of the Honor Code.

For more information about the Mason Honor Code and about the Honor Committee, please visit the website for the Office of Academic Integrity (http://oai.gmu.edu/).

GMU EMAIL ACCOUNTS

Students must use their Mason email account to receive important University information, class-related messages, and to communicate with the professor and the teaching assistants.

See http://masonlive.gmu.edu for more information.

CLASSROOM ETIQUETTE

Cellphones are to be turned off during class; **minimally they must be silenced. Emergency calls may be taken, but must be taken outside of the classroom.**

Texting, using your laptop for something other than lecture-related work, etc. is considered a distraction to me and to the other students trying to learn in the class, and will not be tolerated.

OFFICE OF DISABILITY SERVICES (ODS)

If you are a student with a disability and require special accommodations, please contact me and the Office of Disability Services as soon as possible. All special accommodations must be arranged through ODS.

Office of Disability Services (ODS): (703) 993 – 2474; http://ods.gmu.edu

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OTHER USEFUL CAMPUS RESOURCES

- Writing Center: A114 Robinson Hall; (703) 993 – 1200; http://writingcenter.gmu.edu
- University Libraries: "Ask a Librarian" http://library.gmu.edu/mudge/IM/IMRef.html
- Counseling and Psychological Services (CAPS): (703) 993 – 2380; http://caps.gmu.edu
- The University Catalog: http://catalog.gmu.edu
- University Policies: http://universitypolicy.gmu.edu