GEORGE MASON UNIVERSITY
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
SPRING 2014

ECE 586: DIGITAL INTEGRATED CIRCUIT ANALYSIS AND DESIGN

R 4:30 -7:10 pm --- Aquia Building room #219

Instructor: Dimitris Ioannou, ENG Room # 3248, tel. 993-1580, dioannou@gmu.edu

Office Hours: R 3:00-4:00 pm; plus other times by appointment

Textbook: “CMOS DIGITAL INTEGRATED CIRCUITS”
Rec.: “Chip Design for Submicron VLSI: CMOS Layout and Simulation”
John P. Uyemura (Thomson, 2006)

COURSE OUTLINE

1. MOSFET operation and SPICE modeling
2. CMOS inverters: static characteristics
3. CMOS inverters: dynamic operation
4. Basics of Layout and Design Rules
5. Combinational MOS logic circuits
6. Sequential CMOS logic circuits

Midterm Exam: Thursday 20th

7. Dynamic CMOS logic circuits
8. Differential CMOS Logic Families
9. Semiconductor memories
9. Low Power CMOS

11. Chip input and output circuits
12. Chip design methodologies (intro to ECE 680)

Course Review

Final Exam: Thursday May 8th, 4:30 – 7:10 pm

Grading

Homework / projects - 20%
Midterm - 40%
Final - 40%