ECE 699-001
Digital Signal Processing Hardware Architectures

Course Information

Time and Location: Tuesday 4:30-7:10pm, Robinson Hall, B122
Instructor: Dr. Aaron E. Cohen
Email: acohen8@gmu.edu
Office Hours: Tuesday 3:20-4:20pm, The Nguyen Engineering Building, 3708

Course Description

This graduate course will investigate implementations of digital signal processing algorithms in hardware (including FPGAs and ASICs) and will discuss the use of DSP hardware in modern applications such as mobile phones and wireless LAN. Specifically, the course will investigate:

1. High-level DSP optimizations such as pipelining, unfolding, and parallel processing
2. Common DSP structures such as pipeline FFTs, finite impulse response (FIR) filters, direct digital frequency synthesizers, and correlators
3. Modeling of DSP algorithms in Matlab and conversion of Matlab models into fixed-point VHDL blocks
4. Platform implementation issues: hardware vs. software, FPGA vs. ASIC, power, area, throughput, etc.
5. Applications of DSP hardware such as mobile phones, satellite receivers, and software defined radios

Prerequisites

1. ECE 545, or a demonstrated proficiency with synthesizable VHDL and the Xilinx FPGA flow
2. Undergraduate-level understanding of digital signal processing

More Information

Please email the instructor if you have questions on the prerequisites or have any questions about the course in general.

Textbooks


Supplementary Reading:

Grading

Your course grade will be determined by a combination of homework, presentation, midterm, and final:

- Homework 20%
- Midterm Exam 20%
- Final Exam 30%
- Project 30%

Preliminary Class Schedule

<table>
<thead>
<tr>
<th>Date</th>
<th>Lecture</th>
<th>Chapters</th>
<th>HW</th>
<th>Project</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/21</td>
<td>Course Overview</td>
<td>1,2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1/28</td>
<td>Pipelining and Parallel Processing</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2/4</td>
<td>Retiming</td>
<td>4</td>
<td>1</td>
<td>Selections Due</td>
</tr>
<tr>
<td>2/11</td>
<td>Unfolding</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2/18</td>
<td>Folding</td>
<td>6</td>
<td>2</td>
<td>Fixed Point Software Model Due</td>
</tr>
<tr>
<td>2/25</td>
<td>Systolic Arrays</td>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3/4</td>
<td>Redundant Arithmetic and Numerical Strength Reduction</td>
<td>14, 15</td>
<td>3</td>
<td>Transformation Methods and Block Diagram Due</td>
</tr>
<tr>
<td>3/18</td>
<td>MIDTERM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3/25</td>
<td>Fast Convolution</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4/1</td>
<td>Algorithmic Strength Reduction</td>
<td>9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4/8</td>
<td>Pipelined and Parallel Recursive and Adaptive Filters</td>
<td>10</td>
<td>4</td>
<td>VHDL Logic Completed</td>
</tr>
</tbody>
</table>
Attendance
There is no explicit attendance requirement, but students are expected to attend all courses. If you are absent, you are responsible for turning in homework on time and obtaining class notes from another student.

Homework
Students are required to submit all homework assignments. No late homework will be accepted. Homework assignments are to be completed individually.

Project
Students will work individually on a DSP hardware topic. The list of suggested topics will be given by the instructor on the first day of class. Students will be responsible for performing a literature search, providing a review of prior published works on their topic, selecting or developing a design (or designs), implementing in VHDL, and developing a final report and presentation of their project. The final report should include, but not be limited to, detailed architectural figures, critical path, loop bounds, comparisons to prior work, and area complexity results. The presentation should cover topics in the final report. Students should be prepared to answer questions.

Students with Disabilities
Please talk with me to make arrangements to accommodate your needs.

Honor Code
All rules of the GMU Honor Code system will be in effect. All students should be familiar with the code and abide by its rules. Cheating is taken very seriously. If you violate the honor code, you will be reported to the honor committee and may face sanctions ranging from an F in the course to expulsion from GMU. The honor code (http://www.gmu.edu/catalog/apolicies/#Anchor13) states:

Student members of the George Mason University community pledge not to cheat, plagiarize, steal, or lie in matters related to academic work.