George Mason University  
Volgenau School of Engineering  
Department of Electrical and Computer Engineering

**ECE 331: Digital System Design**  
Syllabus  
Spring 2016

**Professor:** Dr. Craig Lorie  
3221 Nguyen Engineering Bldg.  
clorie@gmu.edu  
(703) 993 – 9616

**Teaching Assistants:**

Lecture: Tuesday / Thursday, 9:00 – 10:15am  
Music/Theater Building, room 1005

**Office Hours:**  
Instructor and TA office hours posted on Blackboard.

**Prerequisites:**  
Grade of C or better in PHYS 260 and 261.

**Corequisites:**  
ECE 332  (Digital System Design Lab)

**Textbook:**  

**Hardware:**  
Digilent Basys2 Board  
http://www.digilentinc.com/

**Software:**  
Xilinx ISE WebPack  
http://www.xilinx.com  
Logisim  
http://www.cburch.com/logisim/index.html

**Class Webpages:**  
https://mymasonportal.gmu.edu/  
(Blackboard)

**Textbook Website:**  

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**Course Description**

This course provides an introduction to the analysis and design of digital logic circuits. It takes a bottom-up approach, using basic logic gates as the fundamental building block, to design simple combinational and sequential logic circuits; these simple logic circuits are then used in the design of more complex digital circuits and systems. The course covers both an historic and a modern design methodology. The historic methodology makes use of Karnaugh maps for circuit simplification and discrete components for circuit realization. The modern methodology implements VHDL for circuit description, CAD tools for design entry and circuit simulation, and PLDs (programmable logic devices) for circuit realization. Equal time is devoted to these two methodologies. The course covers topics ranging from basic logic operations and Boolean expressions through complex Finite State Machines (FSMs). Credits: 3 (Lecture: 3, Lab: 0).

The associated laboratory course (ECE 332) provides practical experience in digital logic circuit design using discrete components, and using VHDL, CAD tools, and PLDs. Credits: 1 (Lecture: 0, Lab: 1).
Learning Outcomes

Following successful completion of ECE 331, the student will be able to:

- Convert between the binary, decimal, and hexadecimal number systems.
- Specify a Boolean equation from a truth table, and construct the truth table for a Boolean equation.
- Minimize Boolean equations using Boolean algebra and Karnaugh maps.
- Analyze combinational logic circuits.
- Design a two-level combinational logic circuit that implements a Boolean equation specified in either of the standard forms – sum of products (SOP) or product of sums (POS).
- Design a minimum-cost combinational logic circuit, given the circuit specification.
- Design multiplexers, decoders, and encoders from basic logic gates.
- Design a one-bit adder from basic logic gates.
- Design a multiple-bit adder/subtractor from one-bit adders and basic logic gates.
- Design latches and flip-flops from basic logic gates.
- Design registers and shift-registers from flip-flops.
- Analyze sequential logic circuits.
- Design counters from flip-flops and combinational logic.
- Design a minimum-cost sequential logic circuit, given the circuit specifications.
- Design complex digital logic circuits and systems from medium-scale building blocks.
- Describe combinational and sequential logic circuits using VHDL (behavioral and structural).
- Write simple VHDL testbenches to simulate and test VHDL designs.

A detailed schedule is provided at the end of this document and posted separately on Blackboard.
CLASS MEETINGS

This course has been designed to improve learning and retention through active participation. Each class meeting will have the following format:

1. Class preparation
   You should review the class materials provided prior to each class meeting. This includes the short presentation (discussed below), the supplemental lecture slides, and any associated reading assignments. The supplemental lecture slides provide greater detail on the topics covered, and should prove to be beneficial when studying for the exams. Proper preparation is essential if you are to be successful in this course.

2. Short presentation
   Through a short presentation, I will provide an overview of the material covered (in each class). I will not review the supplemental slides provided in the lecture materials, but will address any questions on this material.

3. In-class exercises
   The in-class exercises will provide the practice necessary to learn (and retain) the material. Through these exercises, and the active learning process, you will, hopefully, develop a deeper and more complete understanding of the material.

Each in-class exercise will be assigned a point value based on the level of complexity.

<table>
<thead>
<tr>
<th>Type</th>
<th>Points</th>
</tr>
</thead>
</table>
| Review problems  | 0.5 pt.
| Simple problems  | 1 pt.  |
| Complex problems | 2 pts. |

All exercises are multiple-choice. Only a correct answer will earn the points. An incorrect response will earn zero (0) points.

To obtain the full class-participation grade of 5 points (see "Course Grade" section below) you will need to earn 10 points on the in-class exercises during each class meeting. Any points earned beyond the needed 10 points will contribute to extra credit for the class participation grade, with a maximum of 1 additional point.
**I>CLICKER DEVICES**

To facilitate the in-class exercises, this course will use I>clicker devices. The I>clicker2 was chosen because it offers a "self-paced polling" feature which is not available on the other I>clicker devices, nor on the I>clicker mobile app. The "self-paced polling" feature allows you to work on the in-class exercises at your own pace and in the order you choose.

The I>clicker2 device can be purchased from the Bookstore or from the I>clicker website:

https://www1.iclicker.com/products/iclicker-2/

The I>clicker device must be registered at the I>clicker website:

https://www1.iclicker.com/register-clicker/

If you do not register your I>clicker device, your responses will not be properly recorded, and you will not get credit for your participation.

Important information when registering your I>clicker device:

- GMU uses a Learning Management System (Blackboard)
- Your student ID is the prefix of your email address
  (for example, if your email address is xyz@gmu.edu, then your student ID is xyz).
HOMEWORK ASSIGNMENTS

Homework is an essential part of the learning process. Each homework assignment will be composed of:

1. Reading assignment
   The reading assignment will be from the course textbook and/or from supplemental reading sources. The reading will provide greater depth and breadth than can be provided in class. You are expected to complete the assigned reading prior to each class meeting (and before attempting any of the homework problems).

2. Problem set
   The problem set will provide (additional) practice needed to develop a more comprehensive understanding of the material. You are expected to complete, to the best of your ability, all of the assigned problems.

Homework is assigned on a weekly basis (on Blackboard). It will cover the material discussed in class and in the associated reading assignment.

Homework solutions must be submitted via Blackboard. Solutions must be submitted as a single PDF file. You may generate the PDF file directly from a wordprocessor or spreadsheet. Or you may scan your written solutions using a conventional scanner or a scanner app (e.g. Camscan) for your smartphone or tablet. You may not submit pictures of your homework solutions. You are responsible for ensuring that your homework solutions are readable. If the grader cannot read your solutions, they will not be graded and you will receive a zero for your submission.

Homework solutions must be submitted by 5:00pm on the specified due date. Late submissions will be assessed the following penalty:

<table>
<thead>
<tr>
<th>Number of days late</th>
<th>Penalty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5 %</td>
</tr>
<tr>
<td>2</td>
<td>10 %</td>
</tr>
<tr>
<td>3</td>
<td>15 %</td>
</tr>
</tbody>
</table>

Homework solutions will not be accepted more than 3 days late.

You are encouraged to work together on the homework assignments. However, you must submit your own work. Copying any or all of the homework solutions of another student is considered plagiarism and is strictly prohibited. Cheating on a homework assignment will result in a zero (0) for that assignment.

Homework solutions will be graded as follows:

- Two selected problems graded for correctness. 10 pts.
- Remaining problems graded for completeness. 1 pt. each

The lowest homework grade will be dropped at the end of the semester.
Homework solutions must be formatted as follows:

1. Your name should appear at the top-left on all pages of your solutions.
2. The class number (ie. ECE 331) and the assignment number should appear below your name.
3. All pages should be numbered at the top-right.
4. All solutions should be written neatly and clearly.
5. Each problem should be started on a new page (front and back are considered separate pages).
   (Multiple-choice problems may all be included on the same page).

Additional "practice" problems may be included on each homework assignment. These problems do not need to be submitted and will not be graded.
EXAMS

This course includes two Midterm exams and a Final exam. Exam dates are specified in the course schedule.

Each exam will consist of: (1) a set of multiple-choice questions; and (2) several long-answer questions. You must provide a Scantron form for each exam. The specific Scantron form is specified on Blackboard.

The final exam is cumulative.

All exams are closed book. I will provide any necessary reference materials and scrap paper as needed.

If you cannot make one of the scheduled exams, you must speak with me in advance to arrange for an alternate time to take the exam.

RECITATION

The recitation will be conducted by the teaching assistants.

The teaching assistant will provide a brief lecture, at the beginning of each meeting, to supplement the material covered in class. With the remaining time, the TA will work through additional exercises, similar to the in-class exercises and to the homework problems, and answer questions about the homework assignments, class material, and laboratory experiments.

You are responsible for all material covered in recitation. The TA's reserve the right to conduct pop quizzes during recitation. They will not be announced in advance.

A schedule of the topics to be discussed in recitation is provided in a separate document on Blackboard.

DISCUSSION BOARD

All questions about the material covered in this course, including questions about the class, homework assignments, exams, and laboratory experiments, will be addressed using the discussion board on Blackboard (https://mymasonportal.gmu.edu/). Four forums have been created on the discussion board:

1. General questions
2. Homework assignments
3. Exams
4. Labs

Please subscribe to each of the forums – you will then receive an email each time a question or response is posted to one of the forums.

Class-related questions will not be addressed via email. Instead, all questions should be posted to the appropriate forum of the discussion board. Always check the forum before posting your question. The same, or a similar, question may have already been posted (and answered). Furthermore, you may post a "follow-up" question to an existing thread to foster additional discussion and/or to request a more detailed answer.

I will do my best to respond to all questions posted on the discussion board forums. In addition, you may provide a response to any question posted on one of the forums. I will review all answers posted by other students to confirm their correctness.

Any questions or concerns regarding a personal matter should be emailed to me directly. Do not post such comments on the discussion board.
LABORATORY

The laboratory course (ECE 332) consists of a set of experiments to complement the material covered in the lecture course. The majority of the laboratory experiments focus on the use of VHDL (hardware description language), the Xilinx ISE (CAD tool), and the Digilent Basys2 development board, to design, simulate, synthesize, and test combinational and sequential logic circuits. Additional experiments provide experience in circuit design using discrete components, a breadboard, and circuit wiring.

You are expected to be prepared for each lab. This includes review of the associated lecture materials, completion of the associated reading, and, most importantly, completion of the pre-lab. To assess your preparation for the lab, a quiz will be given at the beginning of each lab meeting. You must pass the quiz to receive a full score for the lab. If you fail the quiz:

- the score for the lab will be reduced by 20%.
- no additional time will be provided to complete the lab (beyond the given lab time).
- lower priority will be given to your questions during lab.

You will be expected to complete a lab report for each laboratory experiment.

The laboratory course is administered by the teaching assistants. They will provide additional materials, including a course syllabus, lab schedule, pre-lab requirements, and lab report guidelines. A separate grade will be assigned for the laboratory course by the TAs.

The experiments to be performed include:

0. Lab introduction and overview of laboratory equipment.
1. Binary numbers and binary arithmetic.
2. Verify logical behavior and physical properties of digital logic gates.
3. Design of combinational logic circuits using discrete components.
4. Introduction to the Xilinx ISE and the Digilent Basys2 Development board.
5. Design of a BCD to 7-segment decoder using VHDL.
6. Design of binary adder circuits using VHDL.
7. Design of multiplexers and decoders using VHDL.
8. Design of an arithmetic and logic unit (ALU) using VHDL.
9. Design of a latch, flip-flop, and register using VHDL.
10. Design of a register file using VHDL.
11. Design of a finite state machine (FSM) using VHDL.

Attendance in lab is **required**. Attendance will be taken each week. You will receive a zero (0) for any lab not attended. You will not be allowed to make-up a lab unless you have proper documentation to justify your absence. If you know, in advance, that you will be absent from a lab, please speak with the TA to arrange for an alternate time/date on which to complete the lab.
ATTENDANCE

Class: attendance is not formally recorded. You are, however, responsible for all material covered in class. Furthermore, you cannot earn credit for the in-class problems unless you attend class.

Recitation: you are responsible for all supplementary material covered in recitation. The TA's reserve the right to conduct pop quizzes. These quizzes will not be announced in advance.

Lab: attendance is required and is recorded. You will receive a zero (0) for any lab not attended.

COURSE GRADE

The final grade for the course is based on my best assessment of your understanding of the material and your participation in the class during the semester. The exams, homework assignments, and in-class exercises will be used to determine your final grade according to the following weighting:

<table>
<thead>
<tr>
<th>Component</th>
<th>Weighting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homework</td>
<td>10%</td>
</tr>
<tr>
<td>In-class Exercises</td>
<td>5%</td>
</tr>
<tr>
<td>Midterm Exam #1</td>
<td>25%</td>
</tr>
<tr>
<td>Midterm Exam #2</td>
<td>25%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>35%</td>
</tr>
</tbody>
</table>

The final letter grade will be assigned accordingly.

ACADEMIC INTEGRITY

The George Mason University Honor Code is stated as follows:

"To promote a stronger sense of mutual responsibility, respect, trust, and fairness among all members of the George Mason University community and with the desire for greater academic and personal achievement, we, the student members of the University Community have set for this:

Student members of the George Mason University community pledge not to cheat, plagiarize, steal, and/or lie in matters related to academic work."

You are expected to abide by the Mason Honor Code. Violations of the Honor Code are taken very seriously and will be prosecuted to the fullest extent. This includes, but is not limited to, cheating on homework assignments, quizzes, projects, labs, and exams.

As indicated above, you are encouraged to work together on assessments, and share ideas about solutions to problems. However, you must submit your own work. Copy the solution from another student, or from the author's solution manual, is considered cheating and is a violation of the Honor Code.

For more information about the Mason Honor Code and about the Honor Committee, please visit the website for the Office of Academic Integrity (http://oai.gmu.edu/).
GMU EMAIL ACCOUNTS

Students must use their Mason email account to receive important University information, class-related messages, and to communicate with the professor and the teaching assistants.

See http://masonlive.gmu.edu for more information.

CLASSROOM ETIQUETTE

Cellphones are to be turned off during class; minimally they must be silenced. Emergency calls may be taken, but must be taken outside of the classroom.

Texting, using your laptop for something other than lecture-related work, etc. is considered a distraction to me and to the other students trying to learn in the class, and will not be tolerated.

OFFICE OF DISABILITY SERVICES (ODS)

If you are a student with a disability and require special accommodations, please contact me and the Office of Disability Services as soon as possible. All special accommodations must be arranged through ODS.

Office of Disability Services (ODS): (703) 993 – 2474; http://ods.gmu.edu

OTHER USEFUL CAMPUS RESOURCES

- Writing Center: A114 Robinson Hall; (703) 993 – 1200; http://writingcenter.gmu.edu
- University Libraries: “Ask a Librarian” http://library.gmu.edu/mudge/IM/IMRef.html
- Counseling and Psychological Services (CAPS): (703) 993 – 2380; http://caps.gmu.edu
- The University Catalog: http://catalog.gmu.edu
- University Policies: http://universitypolicy.gmu.edu
# ECE 331: Digital System Design

## Lecture Schedule

<table>
<thead>
<tr>
<th>Date</th>
<th>Lec</th>
<th>Topic</th>
<th>Reading</th>
<th>HW due</th>
<th>Lab</th>
</tr>
</thead>
<tbody>
<tr>
<td>T 1/19</td>
<td>1</td>
<td>Course Introduction</td>
<td>B/V: 1.1 - 1.5</td>
<td></td>
<td>Introduction</td>
</tr>
<tr>
<td>R 1/21</td>
<td>2</td>
<td>Number systems and binary codes</td>
<td>B/V: 1.6, 5.1, 5.7 - 5.8</td>
<td></td>
<td>to ECE 332</td>
</tr>
<tr>
<td>T 1/26</td>
<td>3</td>
<td>Unsigned and signed binary numbers</td>
<td>B/V: 5.1, 5.3</td>
<td></td>
<td>Lab #1:</td>
</tr>
<tr>
<td>R 1/28</td>
<td>4</td>
<td>Binary arithmetic (add, sub, mult)</td>
<td>B/V: 5.2 - 5.3, 5.6</td>
<td>1</td>
<td>Binary Num.</td>
</tr>
<tr>
<td>T 2/2</td>
<td>5</td>
<td>Logic gates; Electrical properties</td>
<td>B/V: 2.1 - 2.4, 3.5, 3.8</td>
<td></td>
<td>Lab #2:</td>
</tr>
<tr>
<td>R 2/4</td>
<td>6</td>
<td>CMOS Logic Circuits</td>
<td>B/V: 3.1 - 3.4, 3.8 - 3.9</td>
<td>2</td>
<td>Logic Gates</td>
</tr>
<tr>
<td>T 2/9</td>
<td>7</td>
<td>Boolean Algebra</td>
<td>B/V: 2.1 - 2.6</td>
<td></td>
<td>Lab #3:</td>
</tr>
<tr>
<td>R 2/11</td>
<td>8</td>
<td>Combinational Logic Design</td>
<td>B/V: 2.6 - 2.8</td>
<td>3</td>
<td>Comb. Logic</td>
</tr>
<tr>
<td>T 2/16</td>
<td>9</td>
<td>Introduction to VHDL</td>
<td>B/V: 2.9 - 2.10, 4.12, A</td>
<td></td>
<td>Lab #4:</td>
</tr>
<tr>
<td>R 2/18</td>
<td>10</td>
<td>Karnaugh Maps 1 (sop)</td>
<td>B/V: 4.1 - 4.2</td>
<td>4</td>
<td>Xilinx ISE</td>
</tr>
<tr>
<td>T 2/23</td>
<td>11</td>
<td>Karnaugh Maps 2 (pos); ISF</td>
<td>B/V: 4.3, 4.4, 2.12, 4.14</td>
<td>5 (EC)</td>
<td>Lab #5:</td>
</tr>
<tr>
<td>R 2/25</td>
<td></td>
<td>Midterm #1 (Lectures 1 - 10)</td>
<td></td>
<td></td>
<td>BCD</td>
</tr>
<tr>
<td>T 3/1</td>
<td>12</td>
<td>Adders</td>
<td>B/V: 5.2 - 5.3, (5.4), 5.5</td>
<td>6</td>
<td>Lab #6:</td>
</tr>
<tr>
<td>R 3/3</td>
<td>13</td>
<td>Multiplier, Comparator, Shifter</td>
<td>B/V: 5.6, 5.9, 6.5</td>
<td></td>
<td>Adders</td>
</tr>
<tr>
<td>T 3/8</td>
<td></td>
<td>No Classes (Spring Break)</td>
<td></td>
<td></td>
<td>No Lab</td>
</tr>
<tr>
<td>R 3/10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T 3/15</td>
<td>14</td>
<td>Multiplexers</td>
<td>B/V: 6.1, 6.6</td>
<td></td>
<td>Midterm</td>
</tr>
<tr>
<td>R 3/17</td>
<td>15</td>
<td>Decoders, Encoders</td>
<td>B/V: 6.2 - 6.4, 6.6</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>T 3/22</td>
<td>16</td>
<td>Structural VHDL; ALU</td>
<td>B/V: A; 6.6.7</td>
<td></td>
<td>Lab #7:</td>
</tr>
<tr>
<td>R 3/24</td>
<td>17</td>
<td>Timing Analysis; Hazards</td>
<td>B/V: 3.8.5; 9.6</td>
<td>8</td>
<td>Multiplexers</td>
</tr>
<tr>
<td>T 3/29</td>
<td>18</td>
<td>Latches, Flip-Flops</td>
<td>B/V: 7.1 - 7.4, 7.12</td>
<td></td>
<td>Lab #8:</td>
</tr>
<tr>
<td>R 3/31</td>
<td>19</td>
<td>Flip-Flops, Registers</td>
<td>B/V: 7.5 - 7.8, 7.12 - 7.13</td>
<td>9</td>
<td>ALU</td>
</tr>
<tr>
<td>T 4/5</td>
<td>20</td>
<td>RAM, ROM, PLDs</td>
<td>B/V: 10.1.3, 6.2.1, 3.6</td>
<td>10 (EC)</td>
<td>Lab #9:</td>
</tr>
<tr>
<td>R 4/7</td>
<td></td>
<td>Midterm #2 (Lectures 11 - 19, excluding Lecture 16)</td>
<td></td>
<td></td>
<td>Flip-Flops</td>
</tr>
<tr>
<td>T 4/12</td>
<td>21</td>
<td>Sequential Logic Analysis</td>
<td>B/V: 8.1, 8.9, 7.15</td>
<td></td>
<td>Lab #10:</td>
</tr>
<tr>
<td>R 4/14</td>
<td>22</td>
<td>Counters</td>
<td>B/V: 7.9 - 7.11, 7.13, 7.8</td>
<td>11</td>
<td>Register File</td>
</tr>
<tr>
<td>T 4/19</td>
<td>23</td>
<td>Sequential Logic Design 1</td>
<td>B/V: 8.1, 8.4, 8.5</td>
<td></td>
<td>Lab #11:</td>
</tr>
<tr>
<td>R 4/21</td>
<td>24</td>
<td>Sequential Logic Design 2</td>
<td>B/V: 8.1, 8.4, 8.5</td>
<td>12</td>
<td>FSM</td>
</tr>
<tr>
<td>T 4/26</td>
<td>25</td>
<td>Sequential Logic Circuits</td>
<td>B/V: 8.2, 8.6</td>
<td></td>
<td>Lab</td>
</tr>
<tr>
<td>R 4/28</td>
<td>26</td>
<td>Asynchronous Sequential Logic</td>
<td>B/V: 9</td>
<td>13</td>
<td>Final</td>
</tr>
</tbody>
</table>