Exam #1: Wednesday, March 2nd, 2011

• Closed book.
• No calculators permitted.
• Show all of your work. Use written English, where applicable. Always write neatly.
• A solution requiring physical units is incorrect if the units are omitted from the result.
• Indicate solution in provided space. If none is provided, underline, circle or box the result.

HONOR CODE PLEDGE:
"On my honor I have neither given nor received aid on this exam"

Your first and last name (printed): ____________________________

Your Signature: ____________________________________________

Failure to sign the pledge may result in no credit for the exam.

Score: ___________ [95]

Score: ___________ [100]
1. [6 pts] Draw the circuit diagram for the following Boolean expression:

\[ F(X,Y,Z) = (X' + Y').Z' + (X Y' + Z')' \]

- Do not simplify or manipulate the expression.
- Use only AND, OR, and NOT gates.
- Logic gates may have any number of inputs.
- For the circuit inputs, simply specify the literal that is needed – i.e. the variable or its complement (e.g. for the complement of X simply write X'); you do not need to include inverters (NOT gates) for the circuit inputs.
2. [6 pts] For the following logic circuit:

\[ F_1 = A B' + A' C \]

(a) Write a Boolean expression for \( F_1 \).

\[ F_1 = A B' + A' C \]

(b) Write a Boolean expression for \( F_2 \).

\[ F_2 = (B + C')(A' + B) \]

\[ F_3 = ((B + C')(A' + B))' \]

\[ = (B + C')' + (A' + B)' \]

\[ F_4 = \]
(c) Write a Boolean expression for \( F_3 \).

\[
F_3 = \left( (B + C') (A' + B) \right)'
\]

\[
= (B + C')' + (A' + B)'
\]

\[
= B'C + AB' = B' (A+C)
\]

(d) Write a Boolean expression for \( F_4 \).

- The expression for \( F_4 \) should be written in either SOP or POS form.
- Only variables should be complemented in the expression for \( F_4 \).
- Sum terms and Product terms should **not** be complemented in the expression for \( F_4 \).

\[
F_4 = F_1 \cdot F_3
\]

\[
F_4 = (AB' + A'C) (B'C + AB')
\]

\[
= AB'B'C + AB'AB' + A'CB'C + A'CB
\]

\[
= AB'C + AB' + A'B'C = AB' + A'B'C
\]

(e) The Boolean expression for \( F_4 \) is in which form? Circle one: SOP POS

\[
AB'C + AB' + B'C = AB' + B'C
\]

\[
F_4 = (AB' + A'C) (B'C + AB')
\]

\[
= (A+A') (A'+B') (A+C) (B'+C) (A+B') (A+C) (B'+B') (B+C)
\]

\[
= (A'+B') (A+C) (B'+C) (A+B') (B') (B'+C)
\]

\[
= (A+C) (B') \leftarrow *10D, \ X(\text{x+y}) = X
\]

\[
\text{POS}
\]
3. [5 pts] Given the following electrical and timing characteristics for a standard logic gate:

<table>
<thead>
<tr>
<th>VCC</th>
<th>VOL</th>
<th>VOH</th>
<th>VIL</th>
<th>VIH</th>
<th>TPLH</th>
<th>TPHL</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 V</td>
<td>0.4 V</td>
<td>2.7 V</td>
<td>0.7 V</td>
<td>2.0 V</td>
<td>12 ns</td>
<td>15 ns</td>
</tr>
</tbody>
</table>

(a) Determine the **voltage range** for a **logic 1** at the **input** of the logic gate. Specify the upper and lower bounds in the space provided.

\[ V_{IH} \rightarrow V_{CC} \]

<table>
<thead>
<tr>
<th>Lower bound</th>
<th>Upper bound</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0 V</td>
<td>5 V</td>
</tr>
</tbody>
</table>

(b) Determine the **voltage range** for a **logic 0** at the **output** of the logic gate. Specify the upper and lower bounds in the space provided.

\[ GND \rightarrow V_{OL} \]

<table>
<thead>
<tr>
<th>Lower bound</th>
<th>Upper bound</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 V</td>
<td>0.4 V</td>
</tr>
</tbody>
</table>

(b) Determine the **propagation delay** of the logic gate corresponding to a **high-to-low** transition on the output of the gate.

\[ t_{PHL} \]

<table>
<thead>
<tr>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 ns</td>
</tr>
</tbody>
</table>
4. [12 pts] Given the following Truth table:

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>F</th>
<th>F'</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

(a) Write the minterm expansion for F in algebraic form.

\[ F = A'B'C' + A'BC + AB'C + ABC' \]

(b) Write the maxterm expansion for F in algebraic form.

\[ F = (A + B + C')(A + B' + C)(A' + B + C)(A' + B' + C') \]

(c) Write the minterm expansion for F' in numeric form.

\[ F' = \sum m(1, 2, 4, 7) \]

(d) Write the maxterm expansion for F' in numeric form.

\[ F' = \Pi M(0, 3, 5, 6) \]
5. [20 pts] Given the following minterm expansion:

\[ F(A, B, C) = \Sigma m(0, 2, 3, 4, 6) \]

(a) Use the Karnaugh map given below to derive the minimum SOP expression.

- Properly label the K-map.
- Show the groups (of 0's or 1's) on the K-map.
- Specify the Boolean expression.

\[ F = A' B + C' \]

(b) Determine the cost of the logic circuit for part (a).

*Hint: Cost = # of logic gates + # of gate inputs.*

\[ \text{Cost} = 2 \text{ gates} + 4 \text{ inputs} = 6 \]

1 2-input AND gate
1 2-input OR gate
Boolean expression from previous page:

\[ F(A, B, C) = \Sigma m(0, 2, 3, 4, 6) \]

(c) Use the Karnaugh map given below to derive the minimum **POS** expression.

- Properly label the K-map.
- Show the groups (of 0's or 1's) on the K-map.
- Specify the Boolean expression.

\[ F = (B + C')(A' + C') \]

(d) Determine the cost of the logic circuit for part (c).

\[ \text{Cost} = 3 \text{ gates} + 6 \text{ inputs} = 9 \]

2 2-input OR gates
1 2-input AND gate.

(e) Which is the "cheaper" circuit? Circle one:  [SOP]  [POS]
6. [16 pts] Given the following maxterm expansion:

\[ F(A, B, C, D) = \Pi M(3, 4, 6, 9, 11, 13). \Pi D(1, 5, 10, 14) \]

Use the Karnaugh map given below to derive the minimum SOP expression.

- Properly label the K-map.
- Show the groups (of 0's or 1's) on the K-map.
- Specify the Boolean expression.

**Karnaugh Map**

Prime Implicants: \( B'D' \), \( AD' \), \( A'BD \), \( BCD \), \( ABC \)

Essential Prime Implicants:

\[ F(A, B, C, D) = B'D' + AD' + BCD \]
7. {20 pts} Design a logic circuit to meet the following specifications:

- The circuit has three inputs: A, B, C
- The circuit has one output: F
- The circuit outputs a
  - **logic 1** for all input combinations that have a decimal equivalent value less or equal to 2 (i.e. \(|ABC| <= 2\)) and greater than or equal to 6 (i.e. \(|ABC| >= 6\)).
  - **logic 0** for all other input combinations.
- The circuit has a minimum cost.

(a) Derive the truth table for the logic circuit:

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
(b) Use the Karnaugh map given below to derive a minimum SOP expression.

\[ F = A'B' + AB + \left\{ \begin{array}{c} BC' \\ A'C' \end{array} \right. \]

\[ \text{Cost} = 4 \text{ gates} + 9 \text{ inputs} \]

\[ \text{Cost} = 13 \]

(c) Use the Karnaugh map given below to derive a minimum POS expression.

\[ F = (A' + B)(A + B' + C') \]

\[ \text{Cost} = 3 \text{ gates} + 7 \text{ inputs} \]

\[ \text{Cost} = 10 \]
(d) Draw the circuit diagram for the minimum cost logic circuit.

- Use only AND, OR, and NOT gates.
- Logic gates may have any number of inputs.
- For the circuit inputs, simply specify the literal that is needed – i.e. the variable or its complement (e.g. for the complement of $X$ simply write $X'$); you do not need to include inverters (NOT gates) for the circuit inputs.

$$F = (A' + B)(A + B' + C')$$

Cost = 3 gates + 7 gate inputs

\[ \Rightarrow 10 \]
8. [10 pts] Simplify the following Boolean expression using **Boolean Algebra**:

- Your final expression should be in **SOP** form.
- The minimum SOP expression will have, at most, 2 product terms, one with 2 literals and one with 3 literals.
  - Full credit will be given to a minimum SOP expression only.
  - Partial credit will be given to all other SOP expressions.
- Use as few steps as possible in the simplification.

\[ F(A,B,C,D) = ABCD + ABCD' + A'B'CD + A'B'D + A'BD + BCD \]

<table>
<thead>
<tr>
<th>Boolean Expression</th>
<th>Theorem / Law</th>
</tr>
</thead>
<tbody>
<tr>
<td>( ABC + A'B'CD + A'B'D + A'BD + BCD )</td>
<td>9</td>
</tr>
<tr>
<td>( ABC + A'B'D + A'BD + BCD )</td>
<td>10</td>
</tr>
<tr>
<td>( ABC + A'B'D + A'BD )</td>
<td>15</td>
</tr>
<tr>
<td>( ABC + A'D )</td>
<td>9</td>
</tr>
</tbody>
</table>

\( [2] \times 3 \) for proper use of **Simplification Theorems**
\( [4] \times 1 \) for proper use of **Consensus Theorem**
\(-2\) for too many steps – to get to correct answer.
\[ F(A,B,C,D) = ABCD + AB\bar{C}D + A'BD + A'BD + BCD \]

\[ = ABC + A'B'CD + A'B'D + A'BD + BCD \]

\[ = ABC + A'B'D + A'BD + BCD \]

\[ = ABC + A'B'D + A'BD \]

\[ = ABC + A'D \]