Multiple-gate SOI MOSFETs

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Abstract

In an ever increasing need for higher current drive and better short-channel characteristics, silicon-on-insulator MOS transistors are evolving from classical, planar, single-gate devices into three-dimensional devices with multiple gates (double-, triple- or quadruple-gate devices). The evolution and the properties of such devices are described and the emergence of a new class of MOSFETs, called triple-plus (3+) gate devices offer a practical solution to the problem of the ultimate, yet manufacturable, silicon MOSFET.

Keywords: SOI; Silicon-on-insulator; MOSFET

1. Introduction

The first SOI transistor dates back to 1964. These were partially depleted devices fabricated on silicon-on-sapphire (SOS) substrates [1]. SOS technology was successfully used for numerous military and civilian applications [2] and is still being used to realize commercial HF circuits in fully depleted CMOS [3–5]. Once the first SOI substrates (the insulator is now silicon dioxide) were available for experimental MOS device fabrication, partially depleted technology the natural choice derived from SOS experience. Partially depleted CMOS continues to be used nowadays and several commercial IC manufacturers have SOI products and product lines such as microprocessors and memory chips. Variations on the partially depleted SOI MOSFET theme include devices where the gate is connected to the floating body. These devices, which have been called “voltage-controlled bipolar-MOS device” [6], “hybrid bipolar-MOS device” [7,8], “gate-controlled lateral BJT” [9], “multiple-threshold CMOS” [10], “dynamic threshold MOS” [11], or “variable-threshold MOS” [12] have ideal subthreshold characteristics, reduced body effect, improved current drive, and superior HF characteristics [13]. They are mostly used for very low-voltage (0.5 V) applications [14]. The first fully depleted SOI MOSFET date back to the early 1980’s where it was quickly established that these devices exhibited superior transconductance, current drive and subthreshold swing [15,16]. In addition to the “regular”, inversion-mode devices it was shown that accumulation-mode FD SOI MOSFETs can be fabricated. These possess characteristics comparable to those of inversion-mode devices [17].

Fig. 1 shows the SOI MOSFETs “family tree”. The first publication describing a double-gate SOI MOSFET dates back to 1984. The device received the acronym XMOS because of the resemblance of the structure with the Greek letter Ξ [18]. This initial paper predicted the good short-channel characteristics of such a device. The first fabricated double-gate SOI MOSFET was the “fully DEpleted Lean-channel TrAnsistor (DELTa, 1989)”, where the silicon film stands vertical on its side (Fig. 2) [19]. Later implementations of vertical-channel, double-gate SOI MOSFETs include the FinFET [20], the MFXMOS [21], the triangular-wire SOI MOSFET [22] and the Δ-channel SOI MOSFET [23]. Volume inversion was discovered in 1987 [24], and the superior transconductance brought about by this phenomenon were first experimentally observed in 1990 in the first practical implementation of a planar double-gate MOSFET called the “gate-all-around” (GAA) device [25] (Fig. 3).
The triple-gate MOSFET is a thin-film, narrow silicon island with a gate on three of its sides. Implementations include the quantum-wire SOI MOSFET [26] and the tri-gate MOSFET [27]. Improved versions feature either a field-induced, pseudo-fourth gate such as the Π-gate device [28] and the Ω-gate device [29] (Fig. 4).

The structure that theoretically offers the best possible control of the channel region by the gate is the surrounding-gate MOSFET. Such a device is usually fabricated using a pillar-like silicon island with a vertical-channel. Such devices include the CYNTIA device (circular-section device, Fig. 5) [30] and the pillar surrounding-gate MOSFET (square-section device) [31].
2. Current drive of multiple-gate SOI MOSFETs

The current drive of multiple-gate SOI MOSFETs is essentially proportional to the total gate width. For instance, the current drive of a double-gate device is double that of a single-gate transistor with same gate length and width. In triple-gate and vertical double-gate structures all individual devices need to have the same thickness and width. As a result the current drive is fixed to a single, discrete value, for a given gate length. To drive larger currents multi-fingered devices need to be used. The current drive of a multi-fingered MOSFET is then equal to the current of an individual device multiplied by the number of fingers (also sometimes referred to as “fins” or “legs”). Considering a pitch \( P \) for the fingers, the current per unit device width is given by:

\[
I_D = I_{D0} \frac{W + 2t_{si}}{P}
\]

where \( I_{D0} \) is the current of a unit-width, planar, single-gate device, and where \( W \) is the width of each individual finger, \( t_{si} \) is the silicon film thickness, and \( P \) is the finger pitch (Fig. 6). The FinFET device achieves high current drive through the use of a relatively thick silicon thickness. In that device there is no current flow at the top of the silicon island, such that \( I_D = I_{D0}(2t_{si}/P) \). In triple-gate devices where \( t_{si} = W \) the finger pitch needs to be smaller than \( 3W \) to obtain a larger current drive than in a single-gate, planar device occupying the same silicon real estate.

3. Short-channel effects

It is possible to predict how small the silicon film thickness should be in multiple-gate devices to avoid short-channel effects (or, at least, to maintain a decent subthreshold swing). Subthreshold swing degradation and other short-channel effects are caused by the encroachment of electric field line from the drain on the channel region, thereby competing for the available depletion charge, and reducing the threshold voltage. The potential distribution in the channel of a fully depleted SOI MOSFET is governed by Poisson’s equation:

\[
\frac{d^2 \Phi(x,y,z)}{dx^2} + \frac{d^2 \Phi(x,y,z)}{dy^2} + \frac{d^2 \Phi(x,y,z)}{dz^2} = \frac{qN_a}{\epsilon_{si}}
\]

Fig. 7 shows how the gates and the drain compete for the depletion charge. Gate control is exerted in the \( y \)- and \( z \)-directions and competes with the variation of electric field in the \( x \)-direction due to the drain voltage.

In the case of a wide single- or double-gate device, \( \frac{d \Phi}{dx} = 0 \), such that we can write:

\[
\frac{d^2 \Phi(x,y)}{dx^2} + \frac{d^2 \Phi(x,y)}{dy^2} = \frac{qN_a}{\epsilon_{si}}
\]

The one-dimensional analysis of a fully depleted device yields a parabolic potential distribution in the silicon film in the \( y \) (vertical) direction. Assuming a similar distribution in the \( y \)-direction for a two-dimensional analysis we can write [32]:

\[
I_D = I_{D0} \frac{W + 2t_{si}}{P}
\]
If we assume that the buried oxide thickness is so large that the potential difference across any finite distance in the BOX is negligible in the y-direction, we can write dΦ(x,y)/dy ≈ 0 in the BOX. Therefore, we have:

\[ c_2(x) \approx -\frac{c_1(x)}{t_{ox}}. \]

Introducing these three boundary conditions in Eq. (4) we obtain:

\[ \Phi(x,y) = \Phi_t(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \Phi_t(x) - \Phi_{gs} \left( -\frac{1}{2t_{si}} \right) \Phi_t(x) - \Phi_{gs} y^2 \]

Substituting Eq. (5) into Eq. (3), and setting y = 0, at which depth \( \Phi(x,y) = \Phi_t(x) \) we obtain:

\[ \frac{d^2 \Phi_t(x)}{dx^2} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \Phi_t(x) - \Phi_{gs} \left( -\frac{1}{2t_{si}} \right) = \frac{qN_d}{\varepsilon_{si}} \]

Once \( \Phi_t(x) \) is determined from Eq. (6), \( \Phi(x,y) \) can be calculated using Eq. (5). Eq. (6), however, can be used for another purpose. If we write

\[ \lambda_1 = \sqrt{\frac{t_{si}}{\varepsilon_{ox}t_{ox}t_{si}}} \]

and

\[ \varphi(x) = \Phi_t(x) - \Phi_{gs} + \frac{qN_d}{\varepsilon_{si}} \lambda_1^2 \]

then Eq. (6) can be written as follows:

\[ \frac{d^2 \varphi(x)}{dx^2} - \frac{\varphi(x)}{\lambda_1^2} = 0 \]

This equation is a simple differential equation with a parameter, \( \lambda_1 \), that controls the spread of the electric potential in the x-direction. Note that \( \varphi(x) \) differs from \( \Phi_t(x) \) only by an x-independent term. Parameter \( \lambda_1 \) is called the “natural length” of the device and it depends on the gate oxide and silicon film thickness. Further analysis and numerical simulations show that the effective gate length of a MOS device must be larger than 5–10 times the natural length to prevent short-channel effects and to produce a reasonable subthreshold behaviour [33].

In the case of a double-gate device the boundary conditions to Eq. (4) are:

1. \( \Phi(x,0) = \Phi_t(x) = \Phi_t(x) = \Phi_t(x) = c_0(x) \) where \( \Phi_t(x) \) is the front surface potential;
2. \( \frac{d\Phi_t(x)}{dx} \big|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\Phi_t(x) - \Phi_{gs}}{t_{ox}t_{si}} = c_1(x) \) where \( \Phi_{gs} = V_{gs} - V_{FBF} \) is the front gate voltage, \( V_{gs} \), minus the front gate flat-band voltage, \( V_{FBF} \).
3. \( \frac{d\Phi_t(x)}{dx} \big|_{y=t_{si}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\Phi_t(x) - \Phi_{gs}}{t_{ox}} = c_1(x) + 2t_{si}c_2(x) = -c_1(x) \) and thus \( c_2(x) = -\frac{c_1(x)}{t_{si}} \).

Substituting these boundary conditions into Eq. (4) yields:

\[ \Phi(x,y) = \Phi_t(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \Phi_t(x) - \Phi_{gs} y \]

\[ -1 \frac{\varepsilon_{ox}}{t_{si}} \Phi_t(x) - \Phi_{gs} y^2 \]

The key difference between this expression and Eq. (5) is that the term \( 1/2t_{si} \) has now been replaced by \( 1/t_{si} \). In other words it looks as if the double-gate device was twice as thin as the single-gate transistor. The natural length of the double-gate device can be derived the same way it was done for the single-gate case, which yields:

\[ \lambda_2 = \sqrt{\frac{t_{si}}{2\varepsilon_{ox}}} \]

The natural length gives a measure of the short-channel effect inherent to a device structure. It represents the penetration distance of the electric field lines from the drain in the body of the device or the amount of control the drain region has on the depletion zone in the channel, as both the gate and the drain compete for that control. A small \( \lambda \) is desired to minimize short-channel effects on the subthreshold slope. Numerical simulations establish that a device is relatively free of short-channel effects if \( \lambda \) has a value smaller than 5–10 times the gate length. The original publication of the natural length concept [33] analyzes single- and double-gate structures. It can be extended to surrounding-gate devices with square cross-section by noting that \( \Phi_{gs} = \frac{d\Phi}{dx} \) in the center of the device, where the encroachment of the electric field lines from the drain on the device body is the strongest. In that case the Poisson equation becomes:

\[ \frac{d^2 \Phi(x,y,z)}{dx^2} + 2 \frac{d^2 \Phi(x,y,z)}{dy^2} - \frac{qN_d}{\varepsilon_{si}} = 0 \]
The thickness/width/diameter can be as large as the gate surrounding-gate structure, where the silicon film the gate length. Further relaxation is obtained using a film thickness is more relaxed and needs to be only half gate length. If a double-gate structure is used, the silicon depleted device needs to be 3–5 times smaller than the thickness of the silicon film in a single-gate, fully gate length. The film thickness requirements for triple-gate, \( \Pi \)-gate and \( \Omega \)-gate devices are located between those for double-gate and surrounding-gate devices. The use of very thin silicon films is thus required for short-channel single-gate devices. However, severe mobility reduction effects have been reported in ultra-thin SOI devices [36–38]. Furthermore, the use of ultra-thin films poses the problem of high source and drain resistance and tight etch selectivity budget. Quite clearly, the use of double-gate, and especially that of surrounding-gate structures, relaxes the requirements on film thickness.

### 4. Triple-plus (3\(^+\))-gate structures

It is quite clear from the above considerations, than the surrounding-gate structure offers the best possible characteristics in terms of current drive and short-channel effects control. All surrounding-gate devices reported in the literature have a vertical-channel and have a non-planar nature, and the source and drain are situated at different depths in the silicon film (Fig. 5). It is, however, possible to design and fabricate quasi-surrounding-gate MOSFETs using a process similar to that used to fabricate triple-gate SOI MOSFETs. Such devices are called either \( \Pi \)-gate [39,40] or \( \Omega \)-gate [41] MOSFETs (Fig. 9). These devices are basically triple-gate devices with an extension of the gate electrode below the active silicon island, which increases current drive and improves short-channel effects. The gate extension can readily be formed by slightly overetching the buried oxide (BOX) during the silicon island patterning step. The gate extension forms a virtual, field-induced gate electrode underneath the device that can block drain electric field lines from encroaching on the channel region at the bottom of the active silicon. Instead the lines terminate on the gate extensions. This gate structure is very effective at reducing short-channel effects. Such devices can be called 3\(^+\) (triple-plus)-gate devices because their characteristics lie between those of triple- and quadruple-gate devices. Fig. 10 presents the equipotential line distribution in (A) a triple-gate, (B) a quadruple-gate, and (C) \( \Pi \)-gate device. The gate length,
silicon film thickness, and width are 30, 50, and 50 nm respectively. The gate voltage and substrate (back gate) voltages are 0V, while the drain voltage is 1 V. Encroachment of electric field from drain on the channel region can be seen in the triple-gate device, but not in the Pi-gate and quadruple-gate devices. These contour plots illustrate the effectiveness of the field-induced, pseudo back gate created by the gate extension. Fig. 11 compares the subthreshold swing of transistors with 2–4 gates with that of a Pi-gate device. Increasing the number of gates improves the subthreshold swing because the control of the channel region by the gate(s) becomes more effective and because multiple gates offer more shielding plates protecting the channel region from the electric field lines from the drain. It should be noted that the performances of the Pi-gate structure are very close to those of a 4-gate device.

These 3+ gate devices offer high current drive and reduced short-channel effects. Unlike classical single- or
double-gate MOSFETs these devices present a non-planar silicon/gate oxide interface involving four corners. Here we will study the influence of these radii of curvature on the device electrical characteristics. It is important to realize that in classical SOI MOSFETs corners appearing at the edge of the device can give rise to parasitic currents which are usually undesirable, while in multiple-gate devices the corners are part of the intrinsic “active” transistor structure. Therefore it is worth understanding the relationship and interaction between currents in the corner and currents in the planar surfaces of the device.

The cross-section of 3+-gate device is shown in Fig. 12. The thickness and width of the device are $t_{si}$; and $W$, and the radii of curvature of the top and the bottom corners are noted $r_{top}$ and $r_{bot}$, respectively. The gate oxide thickness is 2 nm, and $t_{si}$ = $W$ = 30 nm. The depth of the gate extension in the buried oxide, $t_{ext}$, is 10 nm. The gate material is N+ polysilicon with $\Phi_{MS} = -0.9$ V. Because the gate material is N+ polysilicon and the device thickness and width are small, high doping concentrations have to be used to achieve useful threshold voltage values. Fig. 13 presents the $d_{gm}/dV_G$ characteristics of the device at $V_{DS} = 0.1$ V for different doping concentrations and a top and bottom corner radius of curvature of 1 nm. The $d_{gm}/dV_G$ characteristics have been used by several authors to identify the different threshold voltage(s) in accumulation-mode and double-gate SOI devices. The humps of the $d_{gm}/dV_G$ curve correspond to the formation of channels in the device (i.e. they correspond to threshold voltages). The devices with the lowest doping concentrations exhibit a single hump, indicating that both corners and edges build up channels at the same time. The devices with the more heavily doped channels have two humps. The first of these two humps corresponds to inversion in the top corners, and the second one to top and sidewall channel formation. The $dV_G/d(\log(I_D))$ curves of the same devices are shown in Fig. 14. Below threshold the $dV_G/d(\log(I_D))$ values correspond to the subthreshold swing. The more lightly doped devices reach a 60 mV/decade swing for most of the subthreshold current range, while the highly doped MOSFETs barely reach that value. Fig. 15 presents the $d_{gm}/dV_G$ characteristics in a device with a top and bottom corner radius of curvature of 5 nm. In this case a single peak is observed for all doping concentrations, which indicates that premature corner inversion has been eliminated. In that case all devices reach a subthreshold swing of 60 mV/decade over a significant range of their subthreshold current. Further analysis shows that the $d_{gm}/dV_G$ curves of a device with top and bottom corner radii of curvature of 5 and 1 nm, respectively, presents a hump for the highest doping concentrations. This hump is not due to current in the top corners, but rather in the bottom corners.

![Fig. 12. Cross-section of Π/Ω-gate devices. The radii of curvature of the top and bottom corners are $r_{top}$ and $r_{bot}$, respectively; $r_{top} = r_{bot}$ (left) and $r_{top} \neq r_{bot}$ (right).](image)
corners, where inversion channels form at a lower gate voltage than on the other Si/SiO₂ interfaces of the device. The corner effect can thus be eliminated by using either a midgap gate material and low doping concentration in the channel, or corners with a large enough radius of curvature [42,43].

5. Conclusion

Silicon-on-insulator MOS transistors are evolving from the classical, planar, single-gate device into three-dimensional devices with multiple gates (double-, triple- or quadruple-gate devices). These devices offer a higher current drive per unit silicon area than conventional MOSFETs. In addition they offer optimal short-channel effects (reduced DIBL and subthreshold slope degradation). A new class of MOSFETs, called triple-plus (3+)-gate devices offer a practical solution to the problem of the manufacturing surrounding-gate silicon MOSFET. Such structures are three-gate transistors with field-induced, pseudo-fourth gate that emulates a real back (4th) gate underneath the device.

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References

[40] US patent 6,359,311.